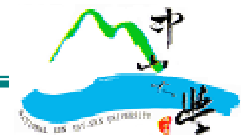


Ansoft 2005 HF/SI/IC/EM Workshop

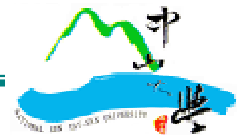
Chip-Package-Board Codesign of W-CDMA RFICs

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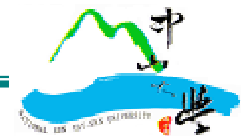
Outline

- | Research motivation
- | Chip-package-board codesign procedure
- | Codesign examples for W-CDMA RFICs
 - ▶ *Upconverter*
 - ▶ *Quadrature modulator*
- | Conclusions

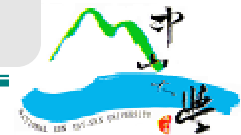
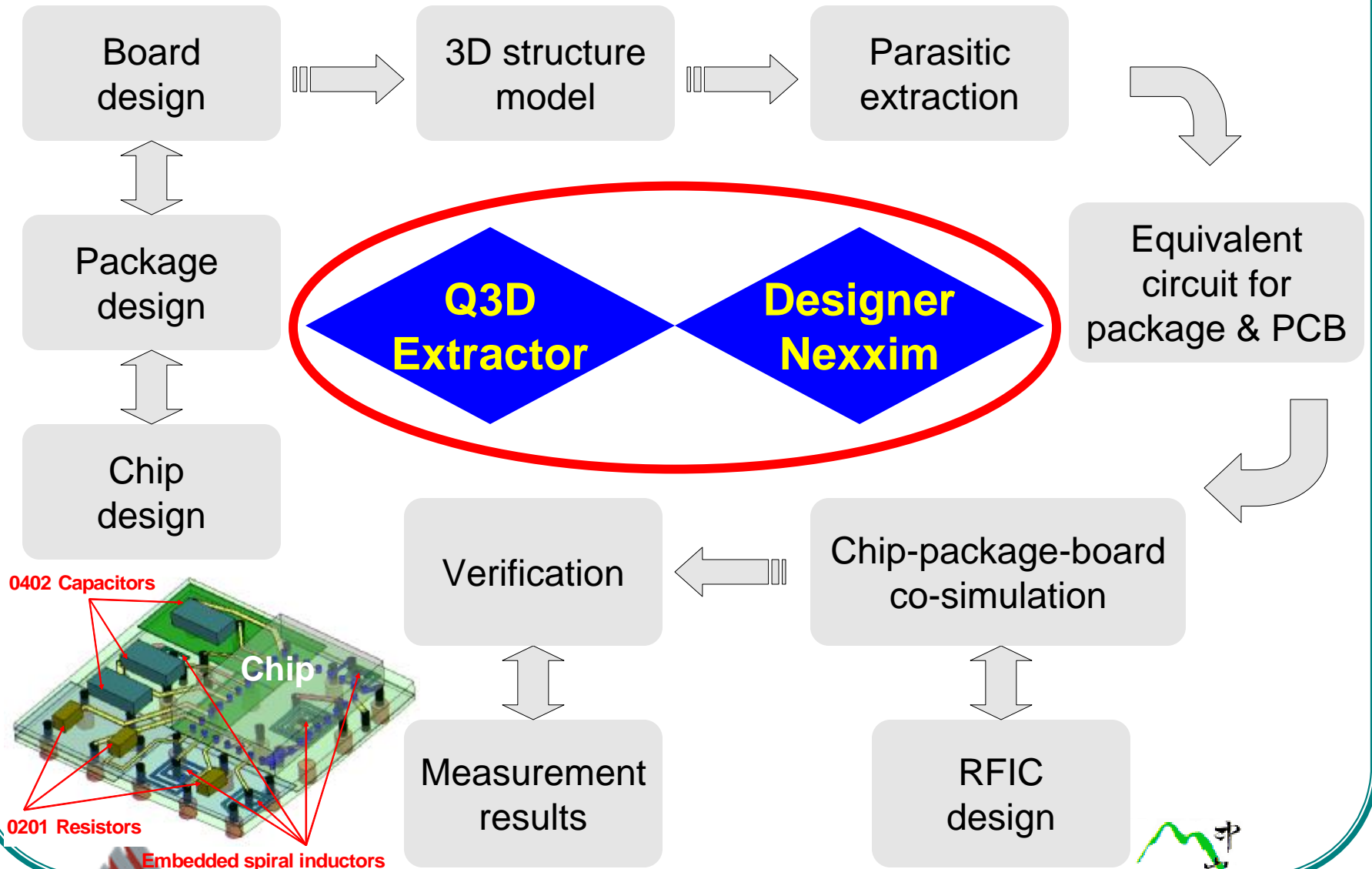


Research Motivation

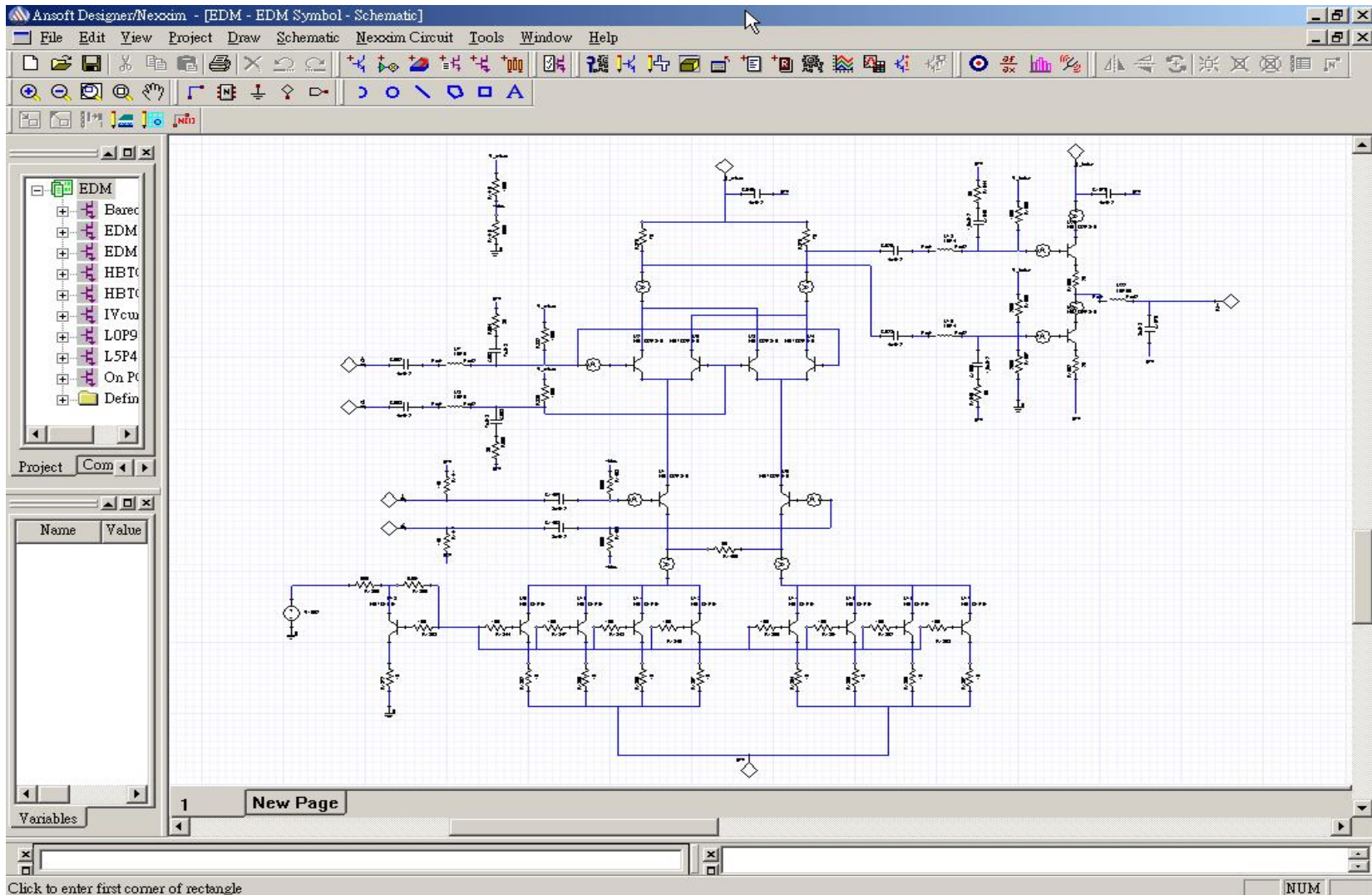
- Most chips need to be packaged and then surface-mounted onto PCB for practical use.
 - The packaged chips operate at higher frequency suffer more from package and PCB effects.
 - A complete procedure for codesign of RFIC, package, and PCB was seldom reported.
- 4 This research aims to propose a general co-simulation procedure for RFICs including the package and PCB effects.



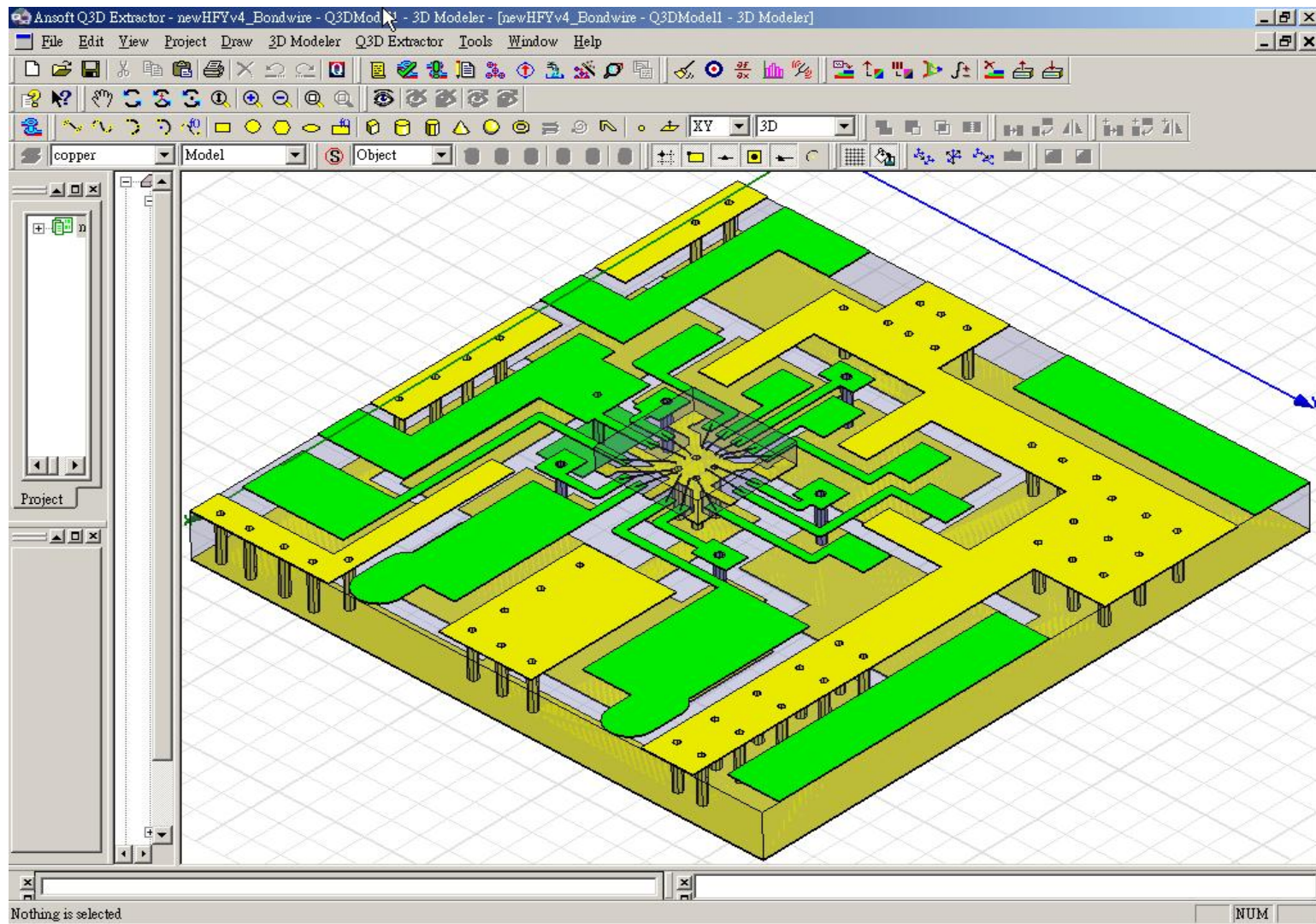
Chip-Package-Board Codesign



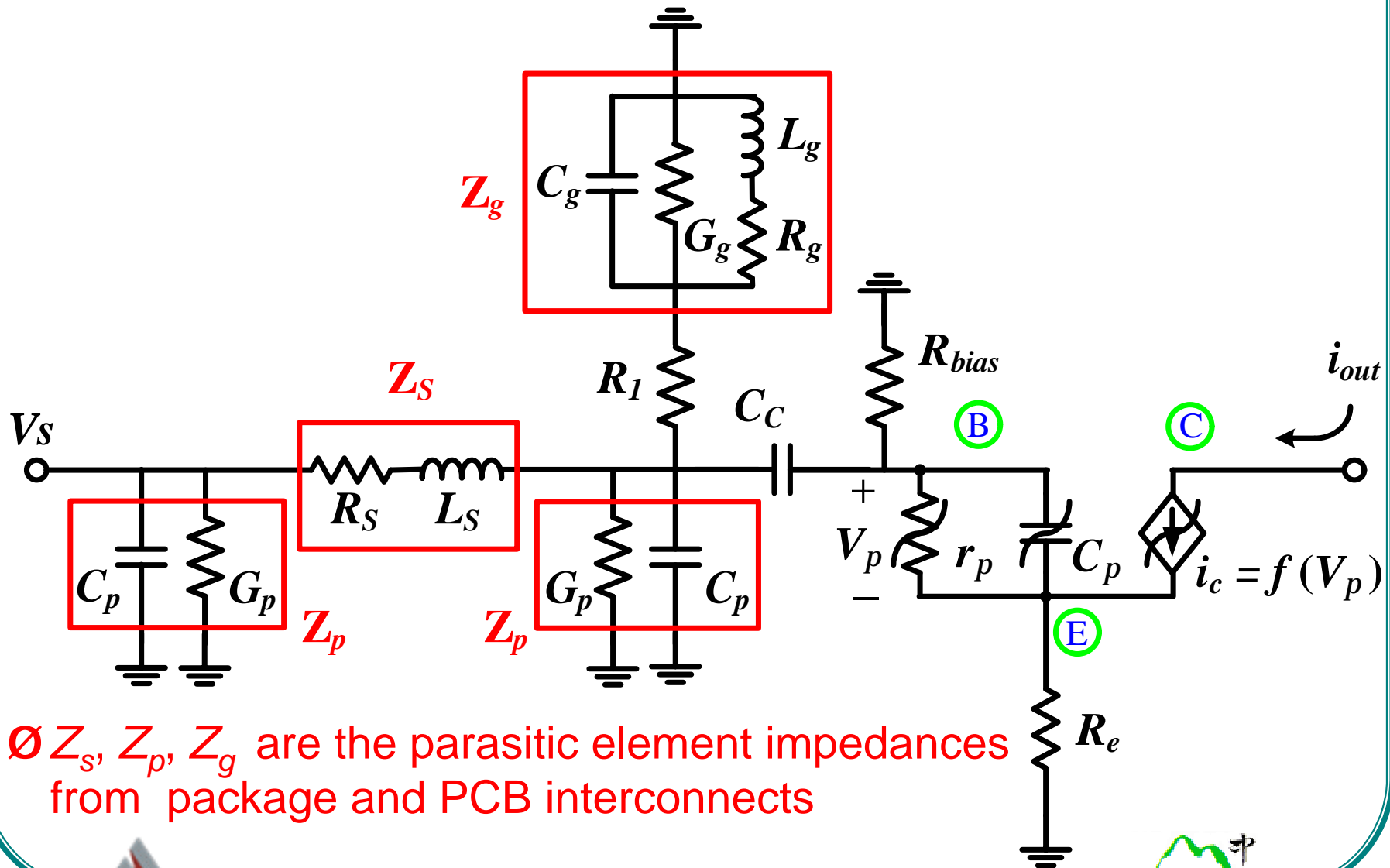
W-CDMA Upconverter RFIC Design



EM Simulation for Package and PCB



Half-Circuit Analysis of the Mixer Stage



$\emptyset Z_s, Z_p, Z_g$ are the parasitic element impedances from package and PCB interconnects

Conversion-Gain Reduction in the Mixer Stage

I Conversion-gain reduction factor

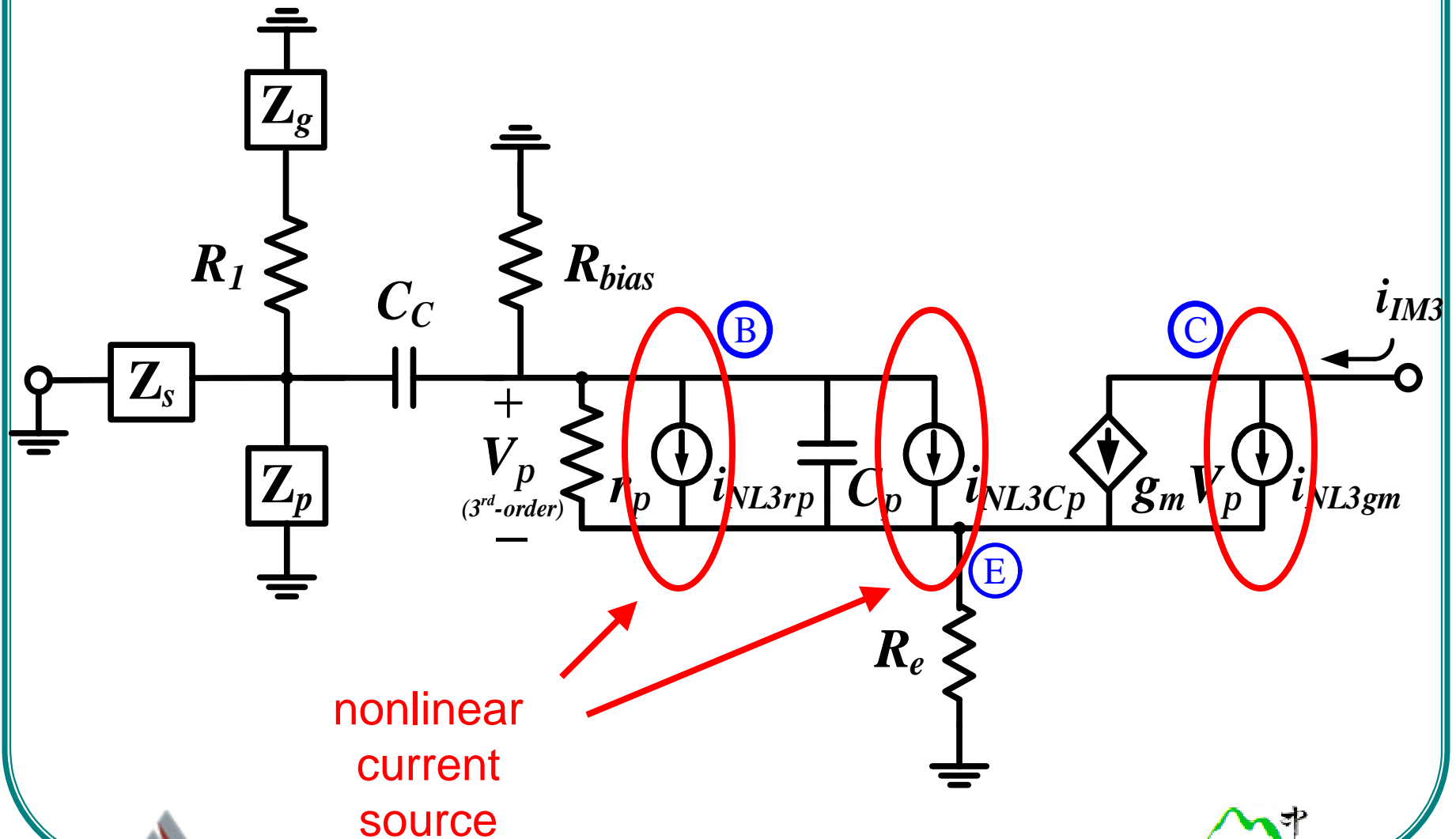
$$G_{r, mixer} = \left(\frac{P_{out, packaged\ chip\ on\ PCB}}{P_{out, bare\ chip}} \right) = \left(\frac{H_{pkg}(s)}{H_{chip}(s)} \right)^2$$

$$= \left(\frac{Z_p \parallel [(Z_{in, base} \parallel R_{bias} + 1/sC_c) \parallel (R_1 + Z_g)]}{Z_s + Z_p \parallel [(Z_{in, base} \parallel R_{bias} + 1/sC_c) \parallel (R_1 + Z_g)]} \right)^2$$

where

$$H_{chip}(s) \triangleq \frac{V_p}{V_S} \Big|_{Z_s, Z_g=0, Z_p=\infty}, \quad H_{pkg}(s) \triangleq \frac{V_p}{V_S} \Big|_{Z_s, Z_g, Z_p \text{ are EM-extracted}}$$

IM_3 Analysis in the Mixer Stage



nonlinear
current
source

OIP₃ Derivation in the Mixer Stage

$$i_{out,(1,0)} = g_m \cdot V_{p,(1,0)}, \quad i_{out,(3,0)} = g_m \cdot K(s) \cdot V_{p,(1,0)}^3$$

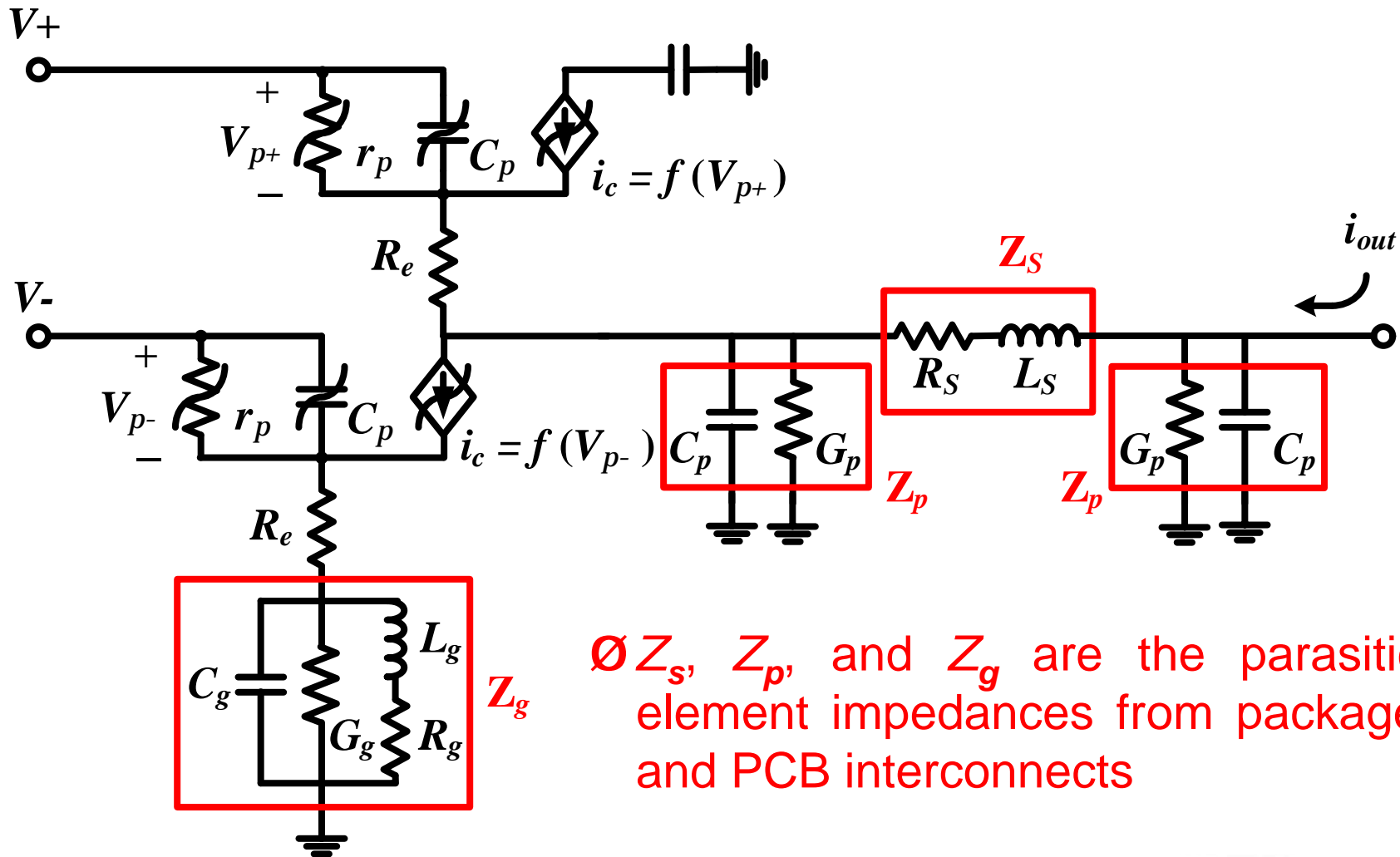
where
$$K(s) = K_{g_m} \frac{K_{g_p} (R_e + Z) + 3 \cdot s \cdot K_{C_p} (R_e + Z) + K_{g_m} R_e}{1 + (g_p + s \cdot C_p)(R_e + Z) + g_m \cdot R_e}$$

$$Z = [Z_s \parallel Z_p \parallel (R_1 + Z_g) + 1/sC_c] \parallel R_{bias}$$

$$i_{out,(2,-1)} = (IMD_3) \cdot i_{out,(1,0)} = (3 \cdot HD_3) \cdot i_{out,(1,0)} \approx 3 \cdot i_{out,(3,0)}$$

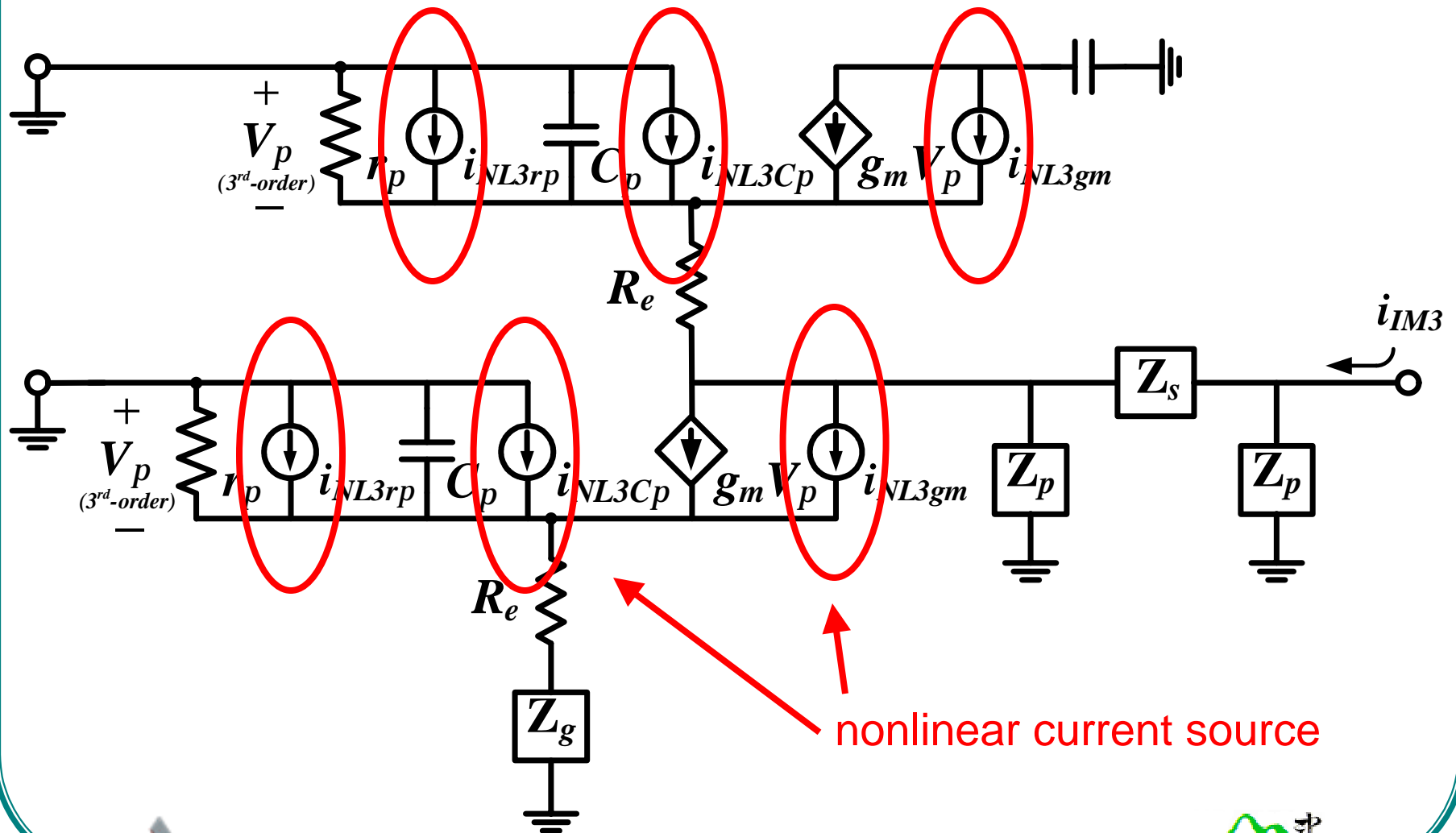
$$\begin{aligned} OIP_{3, mixer} &= [P_{out,(1,0)}^3 / P_{out,(2,-1)}]^{1/2} \\ &= \{ 18 \cdot g_m^{-4} \cdot R_L^{-2} \cdot \left(\frac{R_c}{R_c + Z_L} \right)^{-4} \cdot K(s)^2 \}^{-1/2} \end{aligned}$$

Equivalent Circuit of the Balun Stage



$\emptyset Z_s, Z_p,$ and Z_g are the parasitic element impedances from package and PCB interconnects

IM_3 Analysis in the Balun Stage



Gain Reduction and OIP_3 in the Balun Stage

I Gain reduction factor

$$G_{r, balun} = \frac{P_{out, packaged\ chip\ on\ PCB}}{P_{out, bare\ chip}} = \left(\frac{H_{pkg}(s)}{H_{chip}(s)} \right)^2 \cdot \frac{\text{Re}\{Z_{L, pkg}\}}{\text{Re}\{Z_{L, chip}\}}$$

I OIP_3 derivation

$$OIP_{3, balun} = \left(\frac{9 [A_+(s) H_{p+}^3(s) + A_-(s) H_{p-}^3(s)]}{R_L^2 \cdot H^6(s)} \right)^{-1/2}$$

where

$$H_{chip}(s) \triangleq \left. \frac{i_{out}}{V_{in}} \right|_{Z_S, Z_g=0, Z_p=\infty}$$

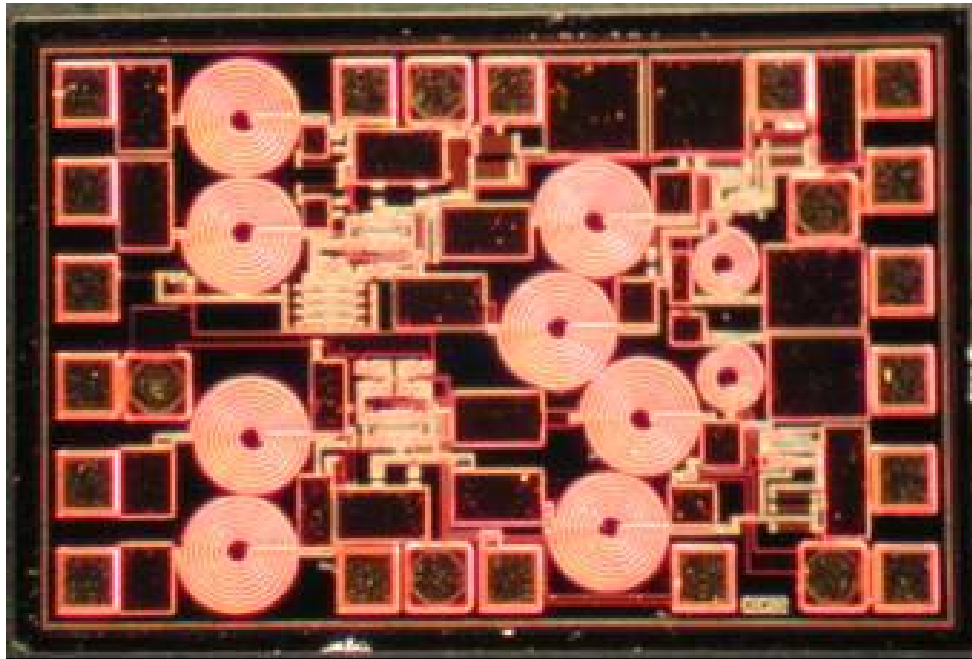
$$A_{\pm}(s) \triangleq \frac{i_{out\pm}(3,0)}{V_{p\pm}^3(1,0)}$$

$$H_{pkg}(s) \triangleq \left. \frac{i_{out}}{V_{in}} \right|_{Z_S, Z_g, Z_p \text{ are EM-extracted}}$$

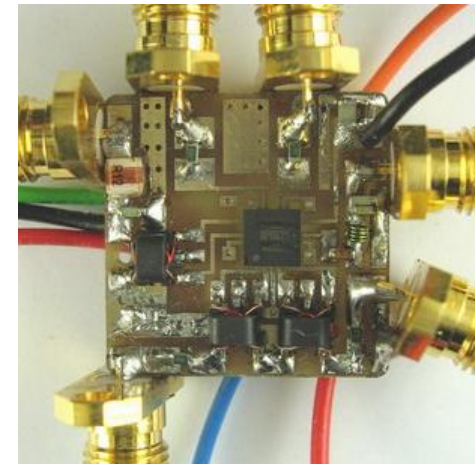
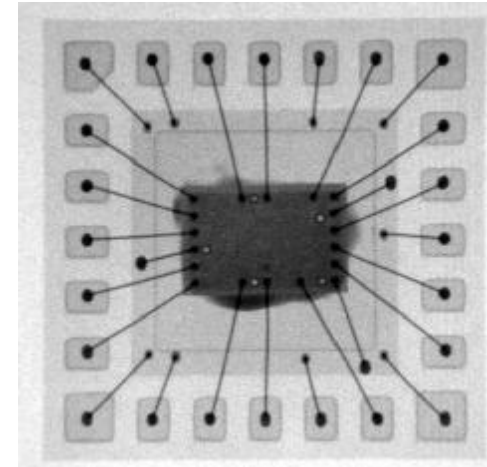
$$H_{p\pm}(s) \triangleq \frac{V_{p\pm}}{V_{in}^+}$$

W-CDMA Upconverter Module Implementation

Chip photo

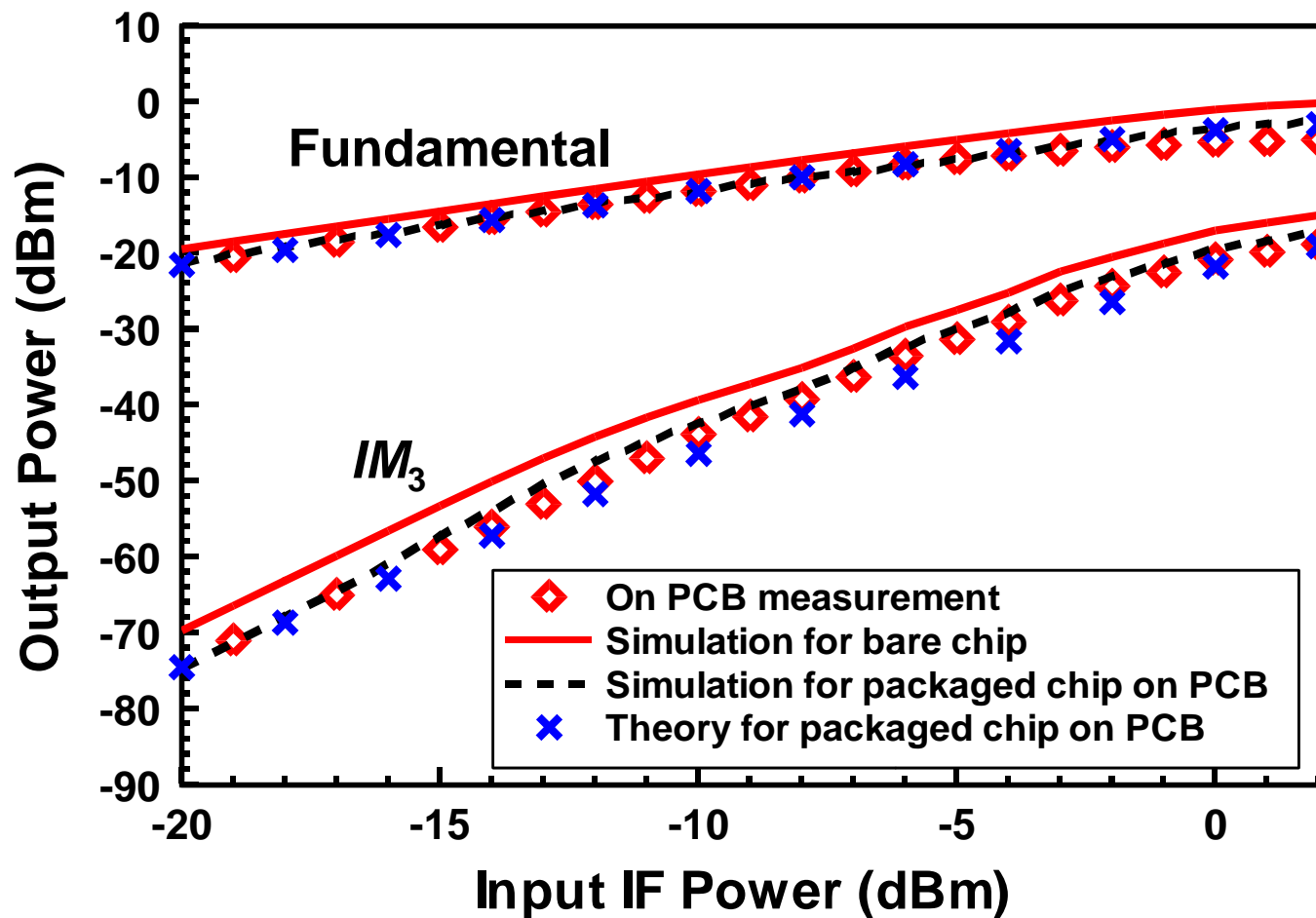


Packaging

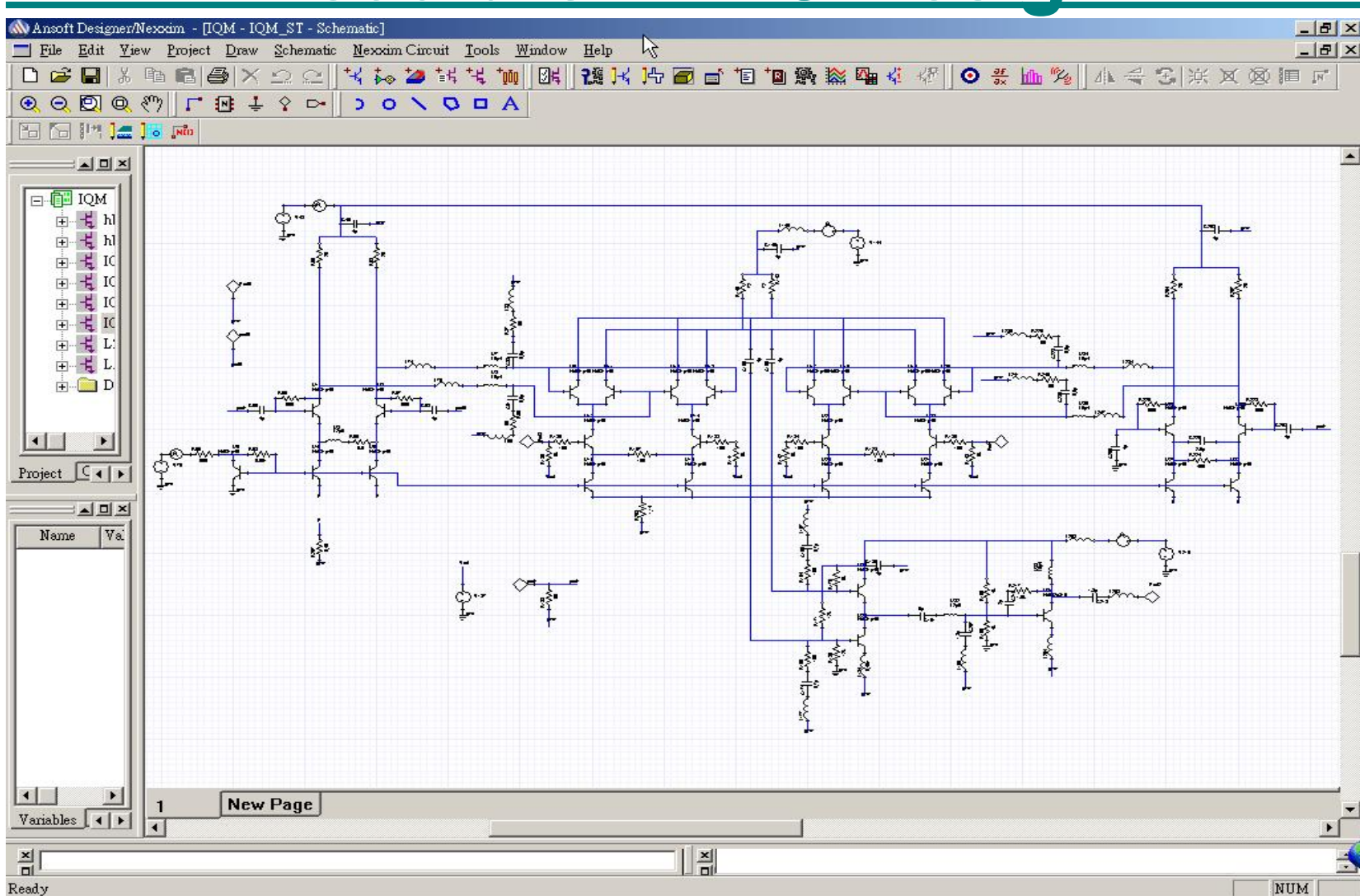


On-board test

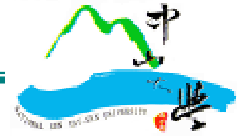
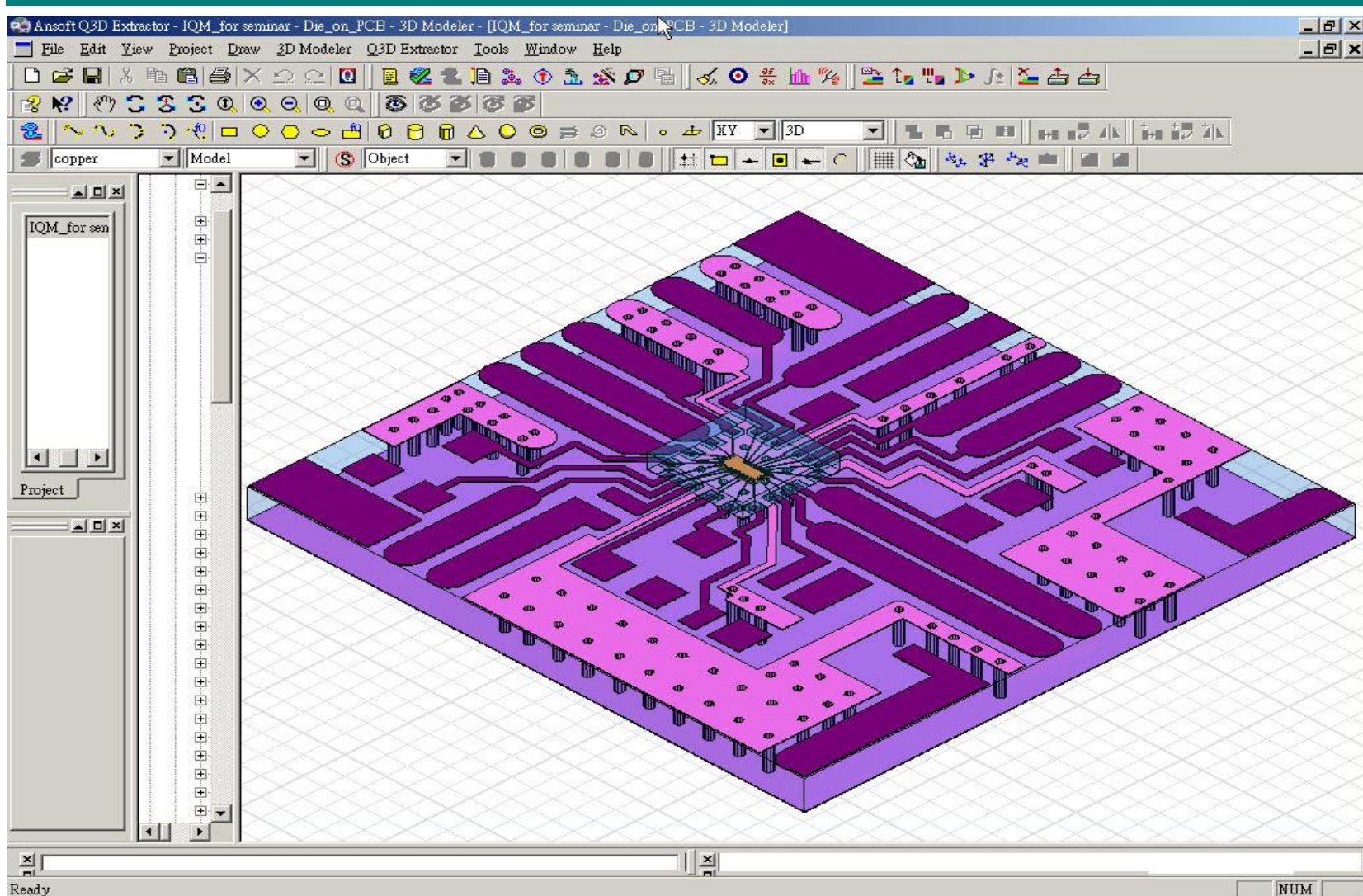
Comparison of Final Results



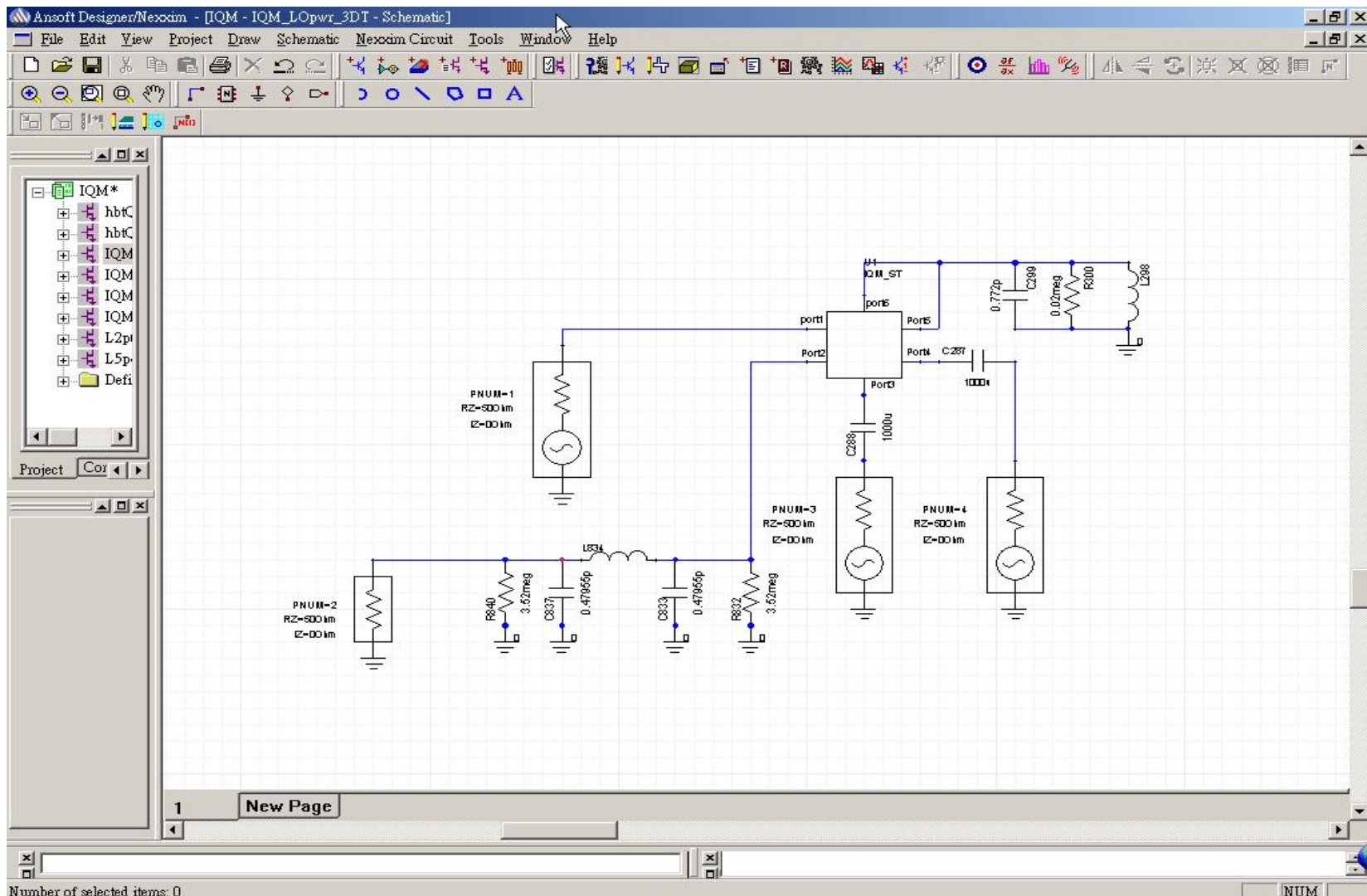
W-CDMA Quadrature Modulator RFIC Design



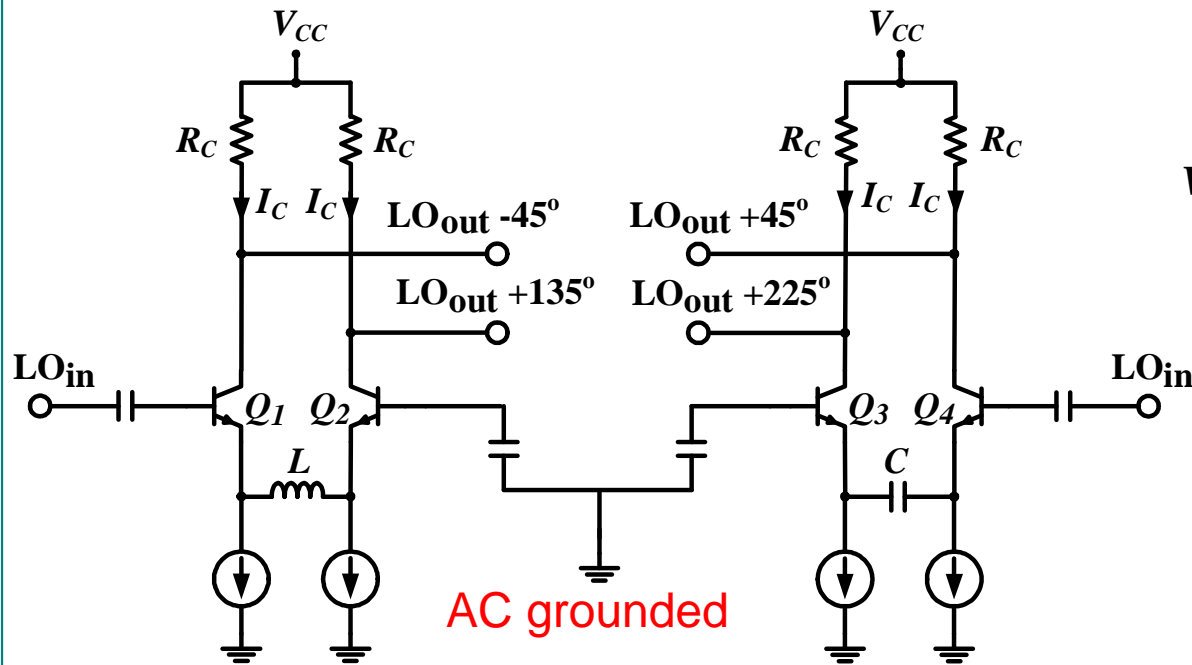
EM Simulation for Package and PCB



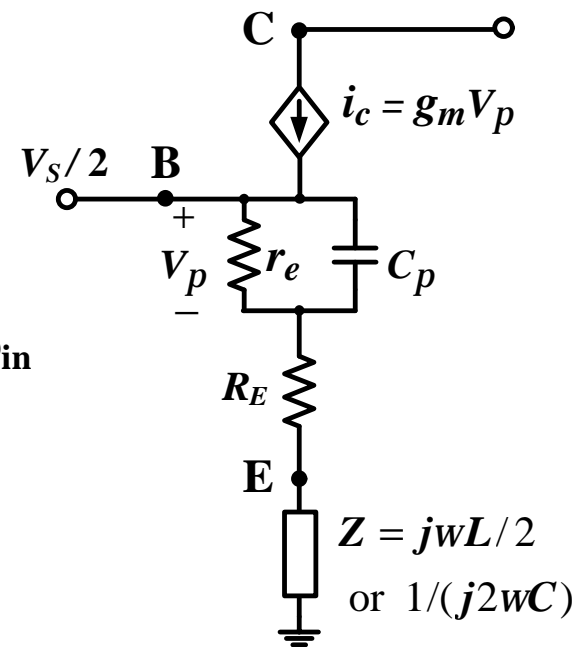
Chip-Package-Board Co-Simulation



New 90-degree Phase Shifter



Circuit schematic



Equivalent differential half-circuit

Amplitude and Phase Imbalances

I Amplitude imbalance

$$A_e(\omega) \approx \left| \frac{2(r_e + R_E) + j\omega L}{2(r_e + R_E) - j/(\omega C)} \right|$$

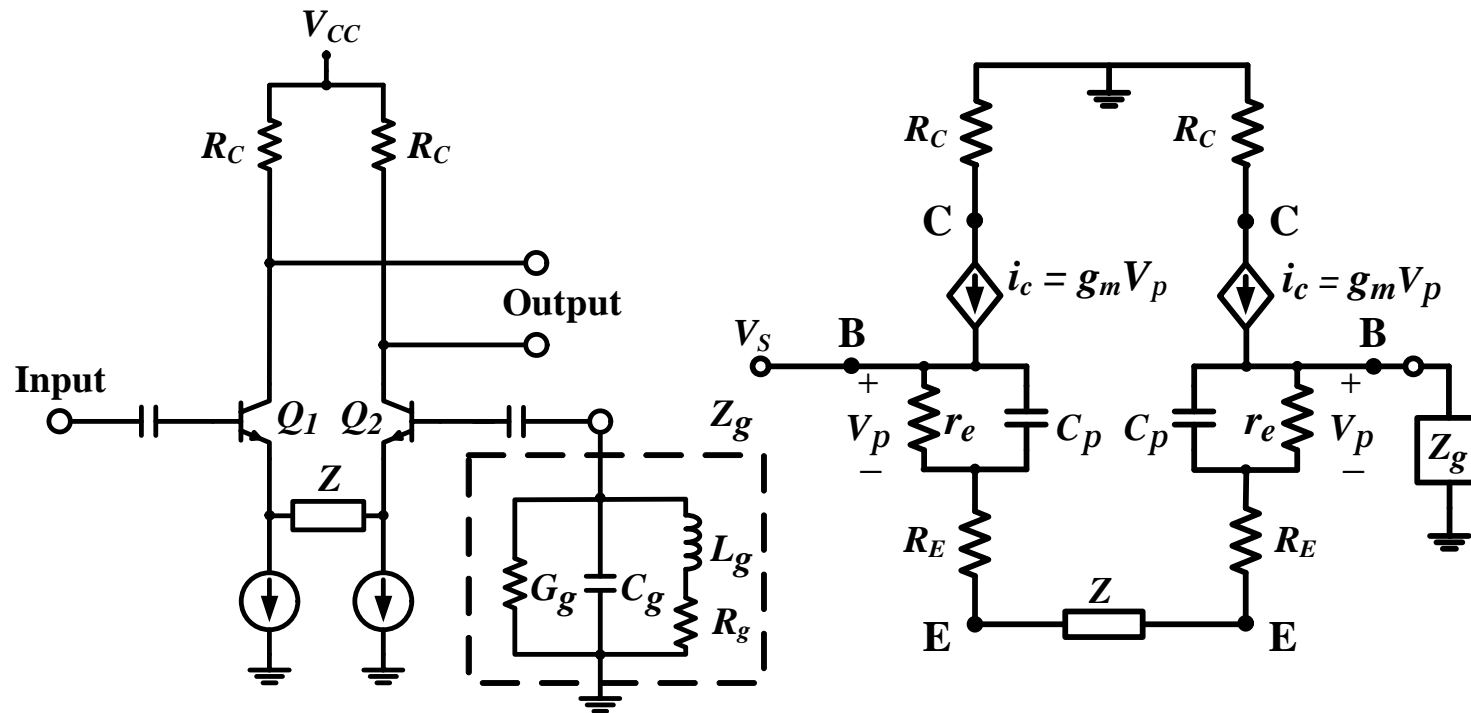
I Phase imbalance

$$q_e(\omega) \approx \tan^{-1} \left[\frac{\omega L}{2(r_e + R_E)} \right] - \tan^{-1} [2(r_e + R_E)\omega C]$$

I Design values for L and C

$$L = \frac{2(r_e + R_E)}{\omega} \quad C = \frac{1}{2\omega(r_e + R_E)}$$

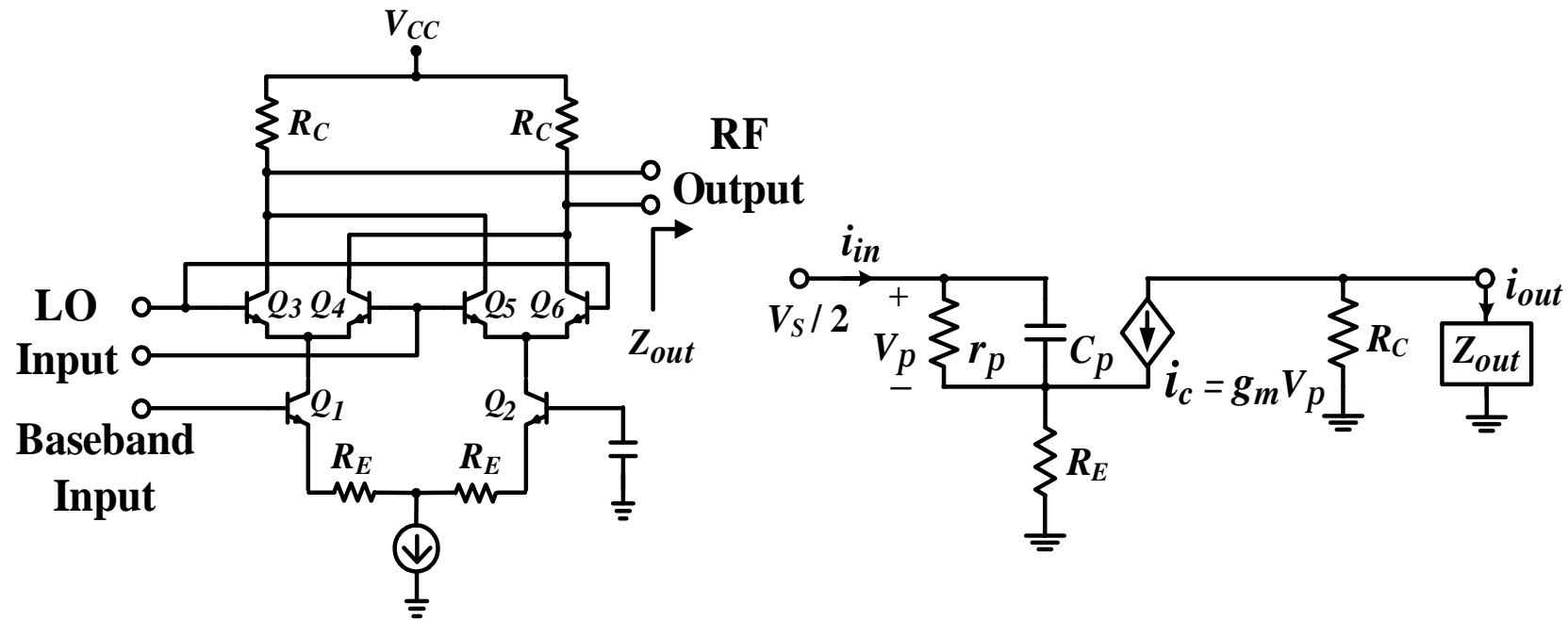
Analysis of 90° Phase Shifter



I Normalized transconductance gain

$$G(\omega) = \frac{i_c}{g_m V_s} = \left[2 + 2(1/r_e + j\omega C_p)(R_E + Z) + Z_g(1/r_e - g_m + j\omega C_p) \right]^{-1}$$

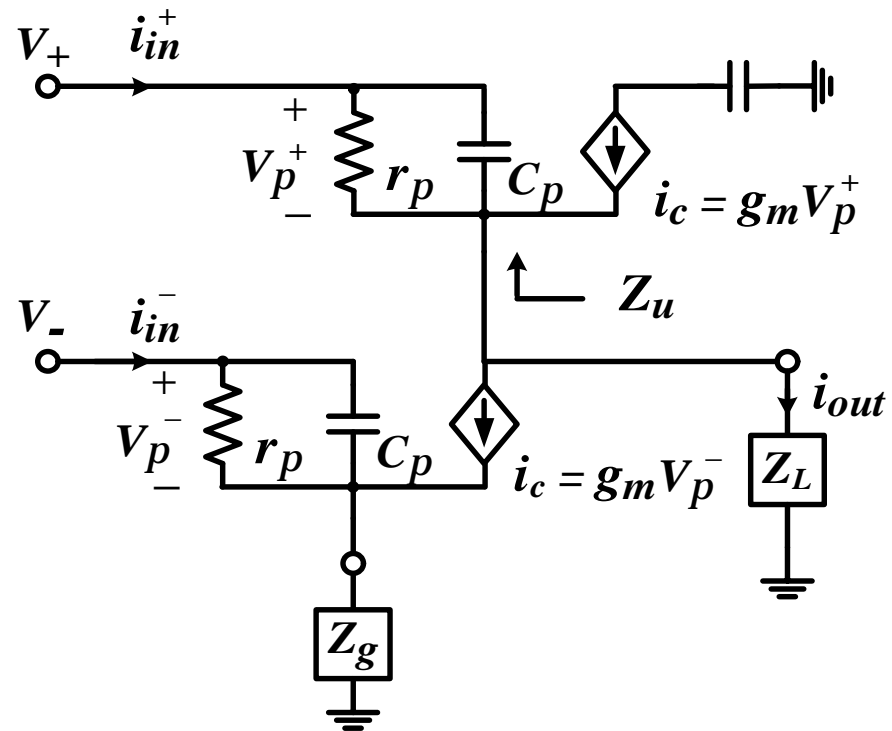
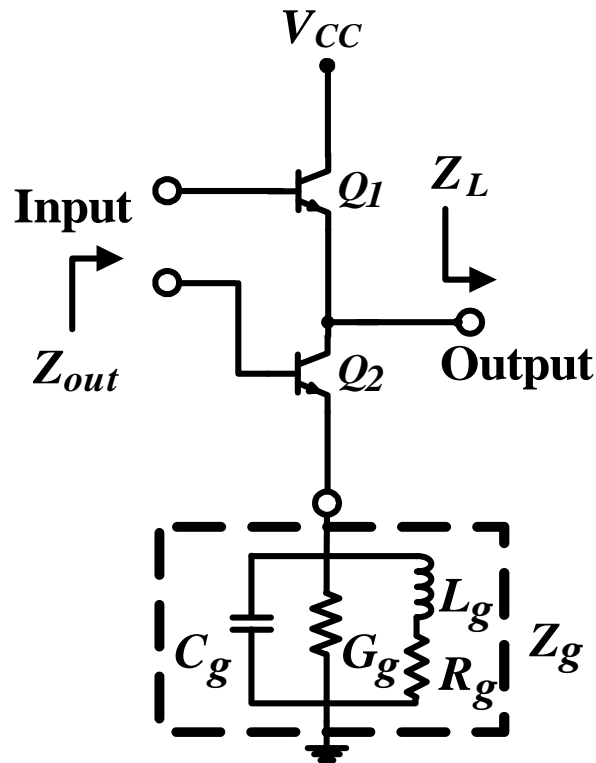
Analysis of Double-Balanced Mixer



I Transconductance gain

$$G(\omega) = \frac{i_{out}}{V_s} = \frac{-2g_m R_C}{\left[1 + R_E \left(\frac{1}{r_p} + j\omega C_p + g_m \right) \right] (R_C + Z_{out})}$$

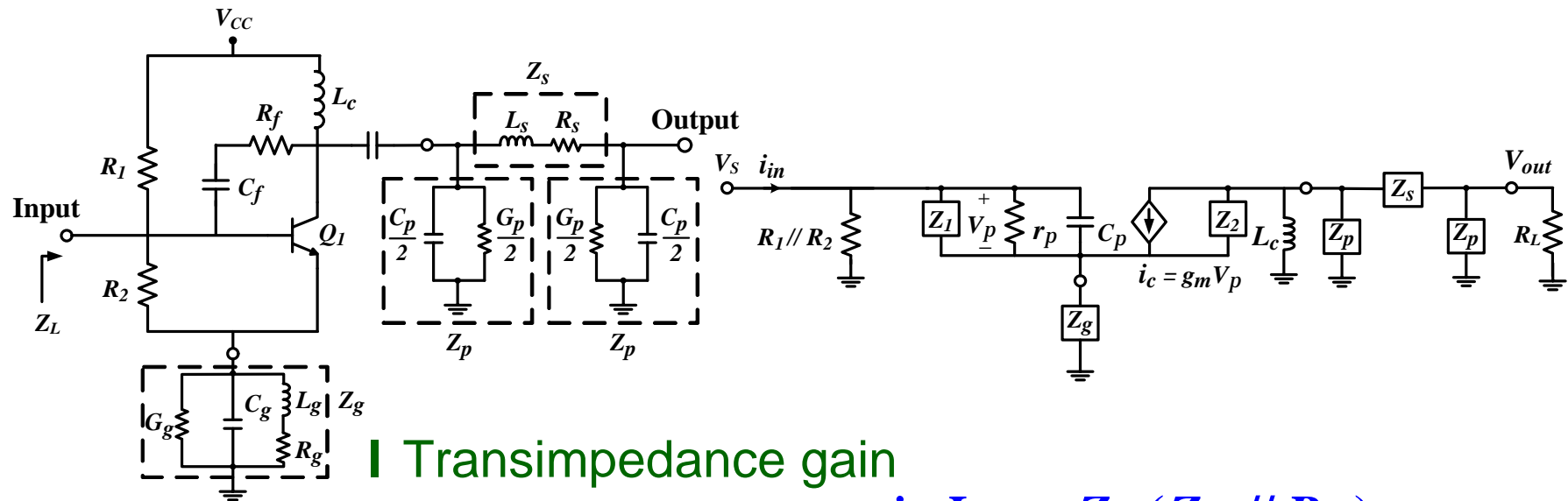
Analysis of Differential to Single-Ended Converter



I Current gain

$$G(\omega) = \frac{i_{out}}{i_{in}} = \frac{i_{out}}{i_{in}^+ + i_{in}^-} = \frac{1/r_p + j\omega C_p + g_m + g_m Z_u / (Z_u + Z_L)}{1/r_p + j\omega C_p}$$

Analysis of Output Buffer



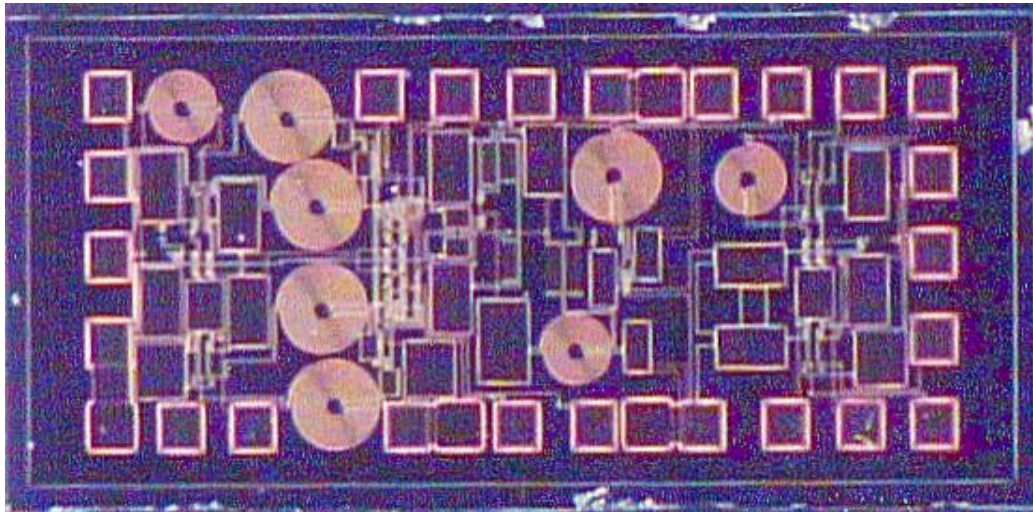
I Transimpedance gain

$$G(\omega) = \frac{V_{out}}{i_{in}} = \frac{-j\omega L_C g_m Z_p (Z_p \parallel R_L)}{j\omega L_C Z_p + (Z_s + Z_p \parallel R_L)(j\omega L_C + Z_p)}$$

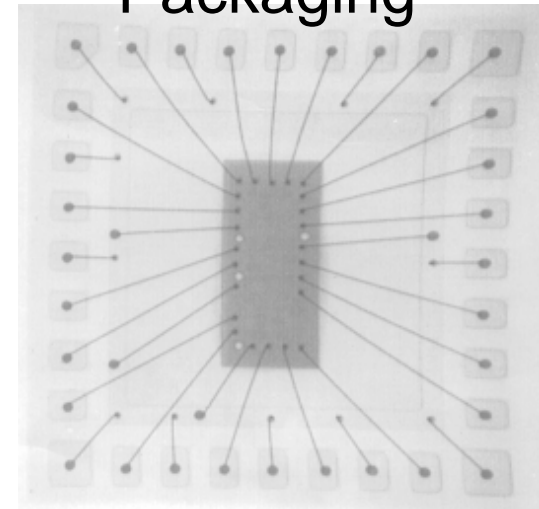
$$g \left[\frac{1 + Z_g \left(\frac{1}{Z_1} + \frac{1}{r_p} + j\omega C_p + g_m \right)}{R_1 \parallel R_2} + \frac{1}{Z_1} + \frac{1}{r_p} + j\omega C_p \right]^{-1}$$

W-CDMA Modulator Module Implementation

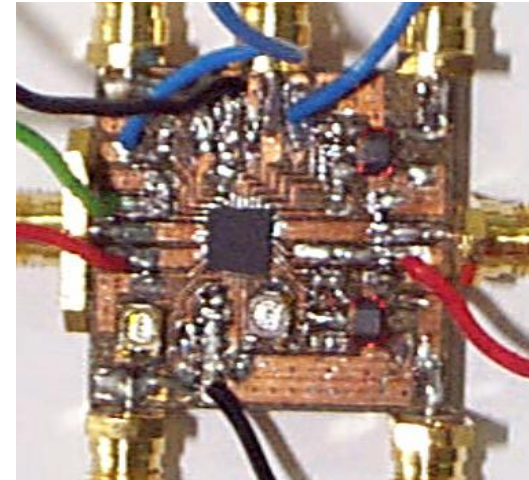
Chip photo



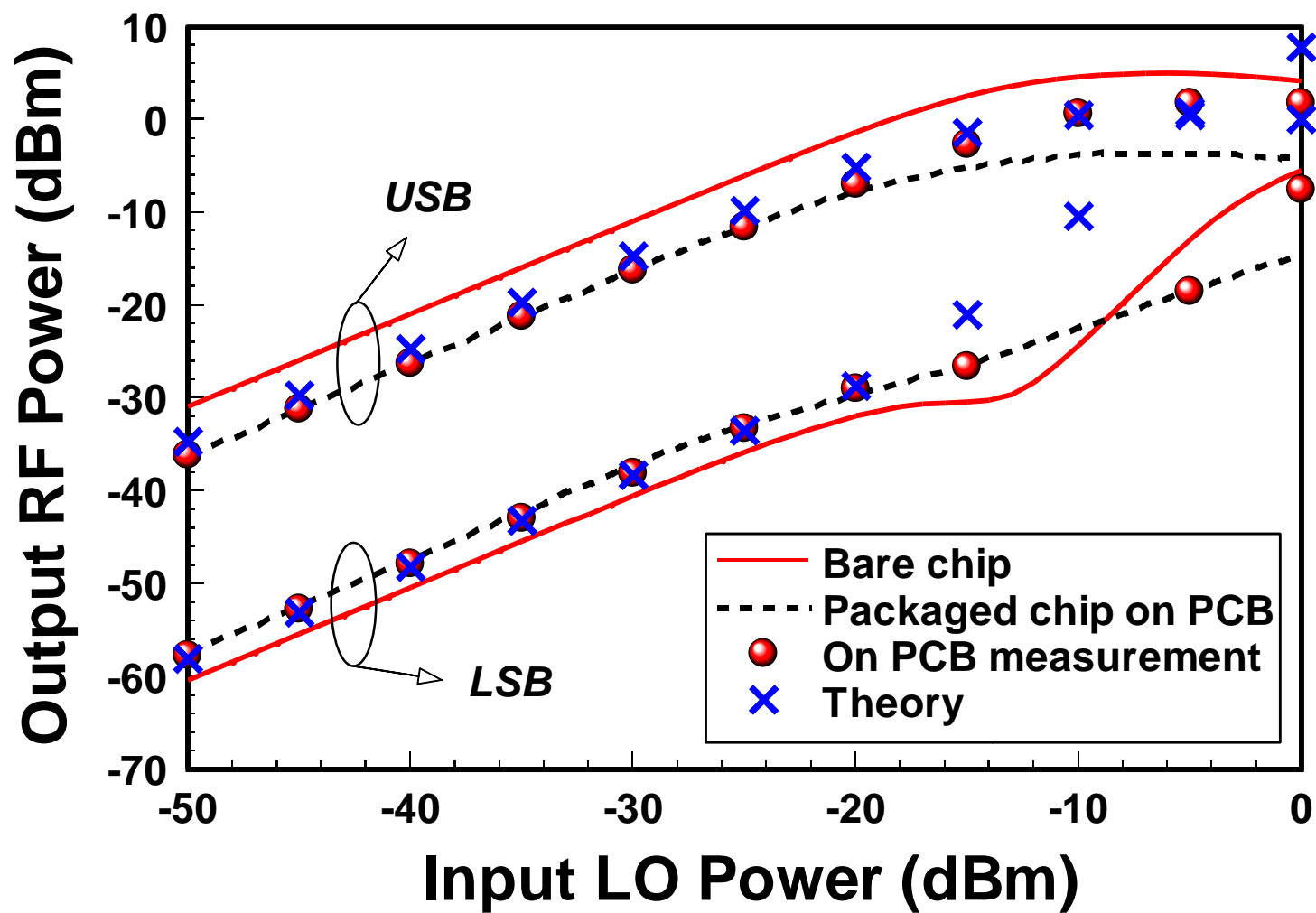
Packaging



On board test



Comparison of Final Results



Conclusions

- Practical chip-package-board codesign examples are demonstrated in implementing the W-CDMA RF component modules.
- The package and PCB interconnects are transformed into the equivalent circuit elements using Q3D extractor for co-simulation with RFICs in Nexxim simulator.
- For both realized modules, the co-simulation results agree quite well with our theoretical predictions as well as the final measurements.