

Steady State, Stability and Transient Analysis of a Sync-Buck DC/DC Converter

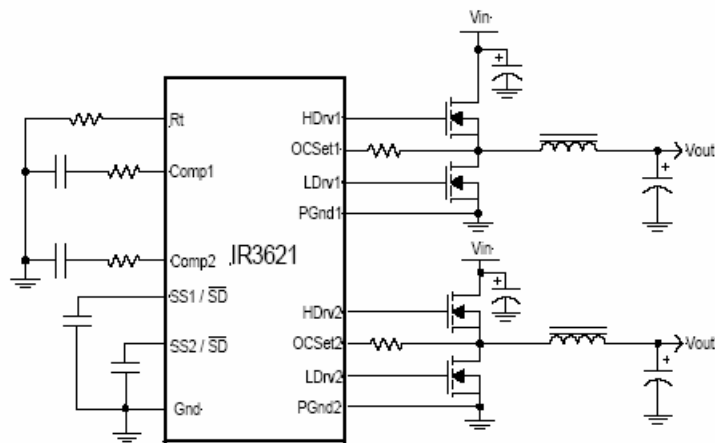
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Agenda

- **What is DC/DC conversion?**
- **Overview of a DC/DC circuit**
- **Steady State analysis**
 - Transient run
 - Efficiency sweep
- **AC and Transient Response Analysis**
 - AC analysis
 - Bode Plot
 - Phase Margin
 - Monte Carlo
 - Phase Margin
 - Load Current Step Response
- **Conclusion**

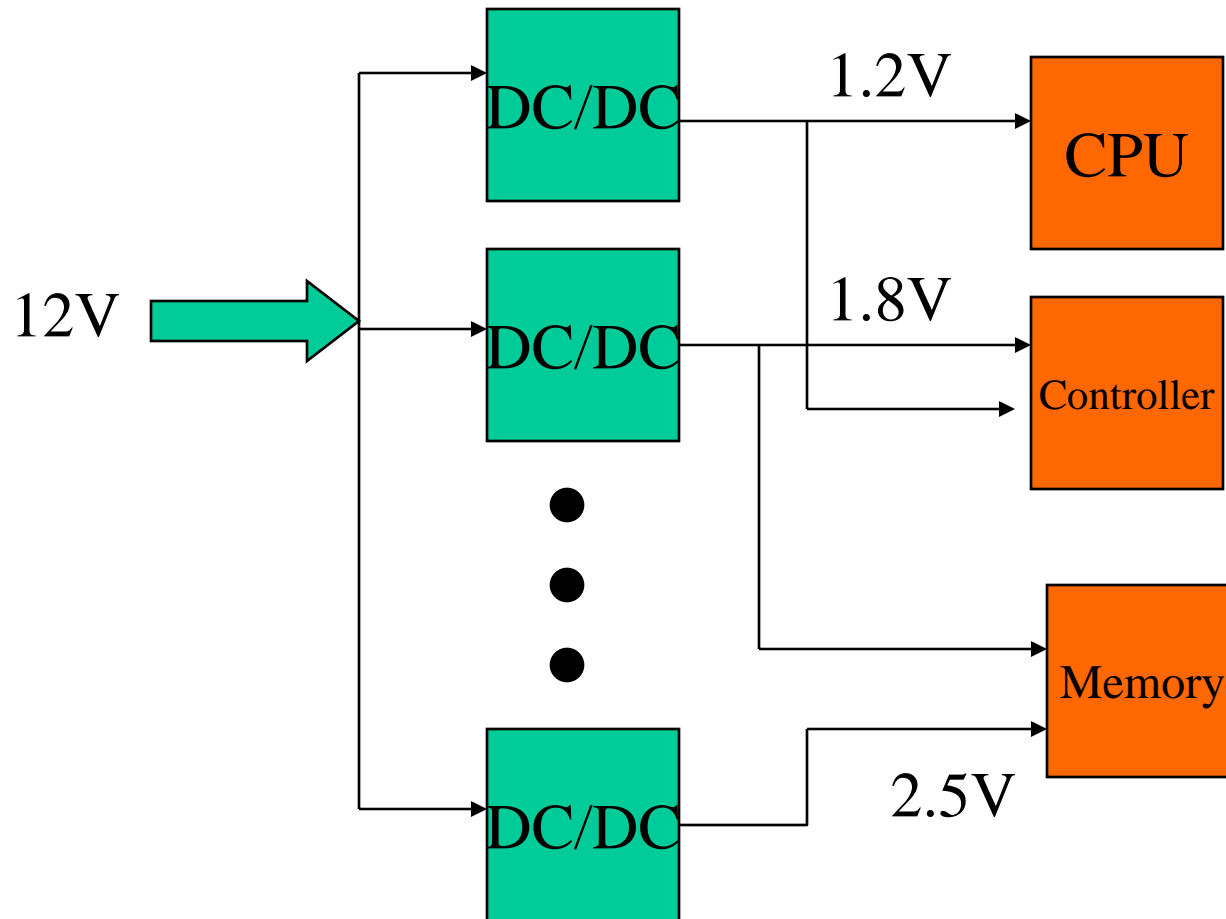
DC/DC Conversion

- **Circuit boards with digital devices usually require a step down voltage conversion.**
- **Usually the voltage supplied to the board is 12V DC.**
- **Each digital device CPU, RAM, Flash, Bus Controller, etc. requires a tightly regulated input voltage.**
- **A Sync-Buck (step down) converter topology is used.**
- **Output currents range from 5A to 200A**

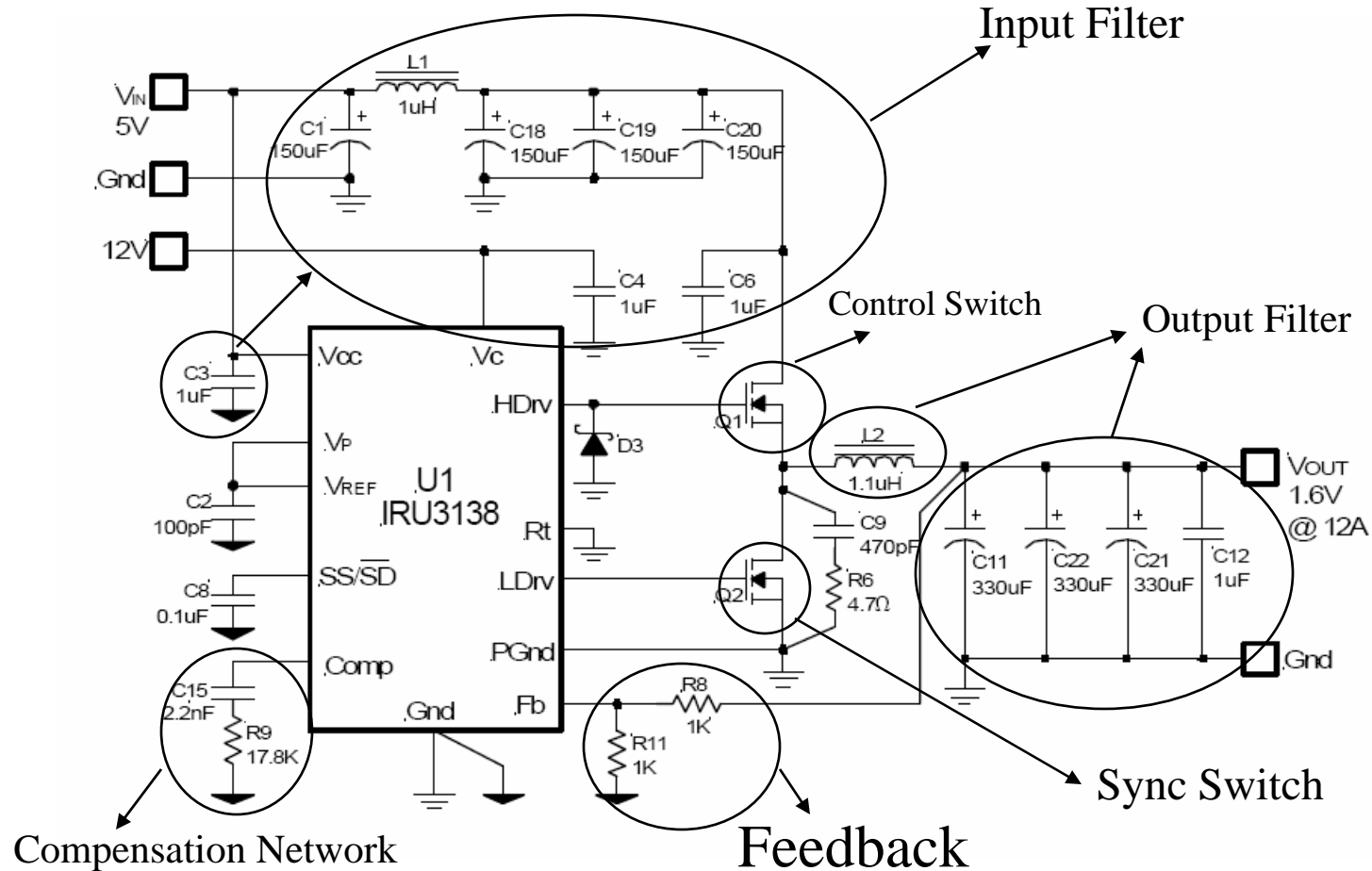


DC/DC Conversion

Example Point of Load Scheme



Sync_Buck Circuit



Steady State Analysis

- **Purpose**

- Verify the design against input design parameters
- Evaluate steady state waveforms in the circuit
 - Gate voltages
 - Effect of deadtime
 - Reverse recovery effects
 - Switch node
 - Etc
- FET power dissipation estimate
- Overall efficiency estimate

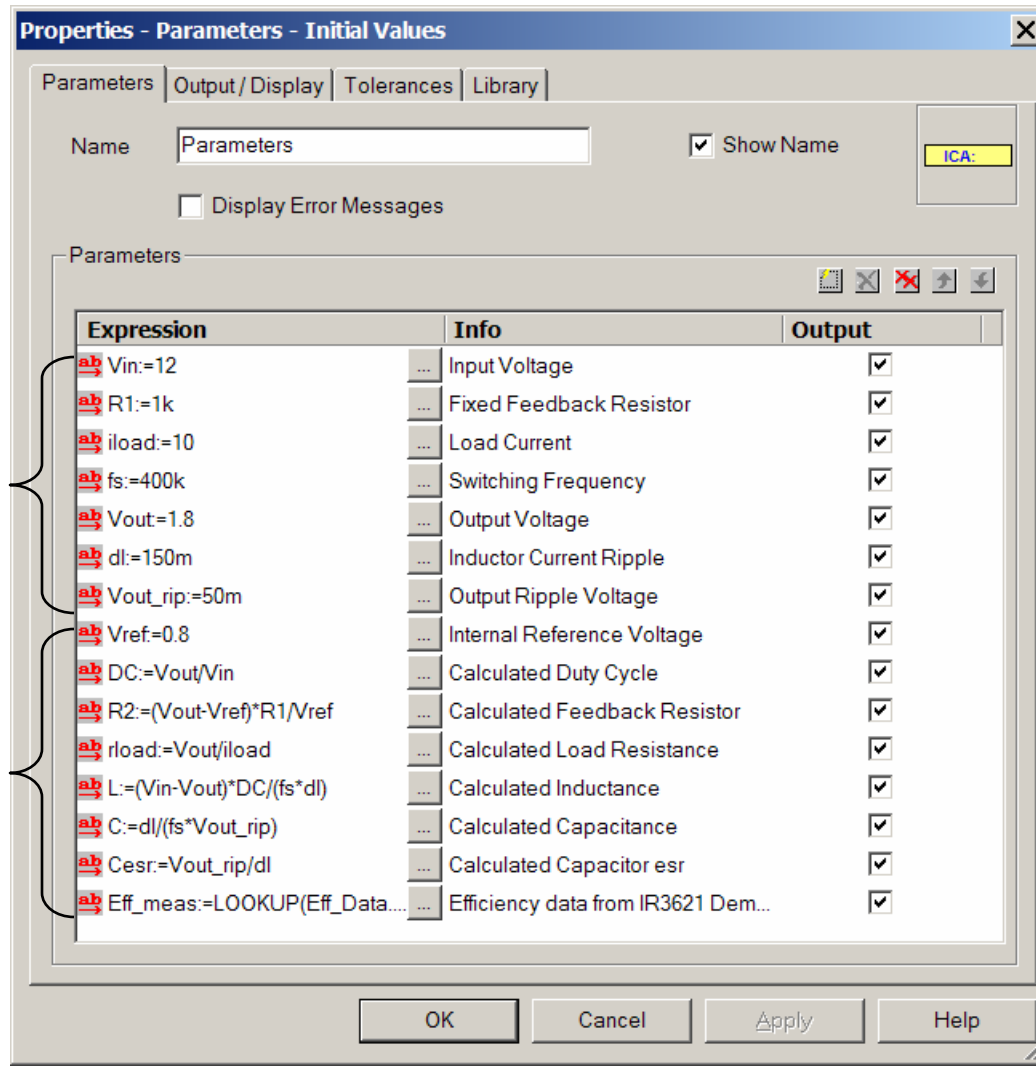
- **Limitations**

- Slow simulation times
- Thermal consideration not taken into account (In this case not modeled however thermal effects can be added)

Steady State Model of Sync-Buck Application

- **Design Input Parameters**
 - V_{in} => Bus voltage
 - V_{out} => Output voltage
 - ΔI => Inductor ripple current
 - ΔV => Output ripple voltage
 - f_s => Switching frequency
 - V_{ref} => Controller IC's internal reference voltage
 - R_1 => Pull down resistor in the feedback network
- **Calculated Design Parameters**
 - DC => Steady state duty cycle
 - R_2 => Second resistor in feedback network
 - L => Main inductor
 - C => Main capacitor
 - C_{esr} => Main capacitor's esr
 - R_{load} => Load resistance
 - Eff => Circuit efficiency at a given output load current

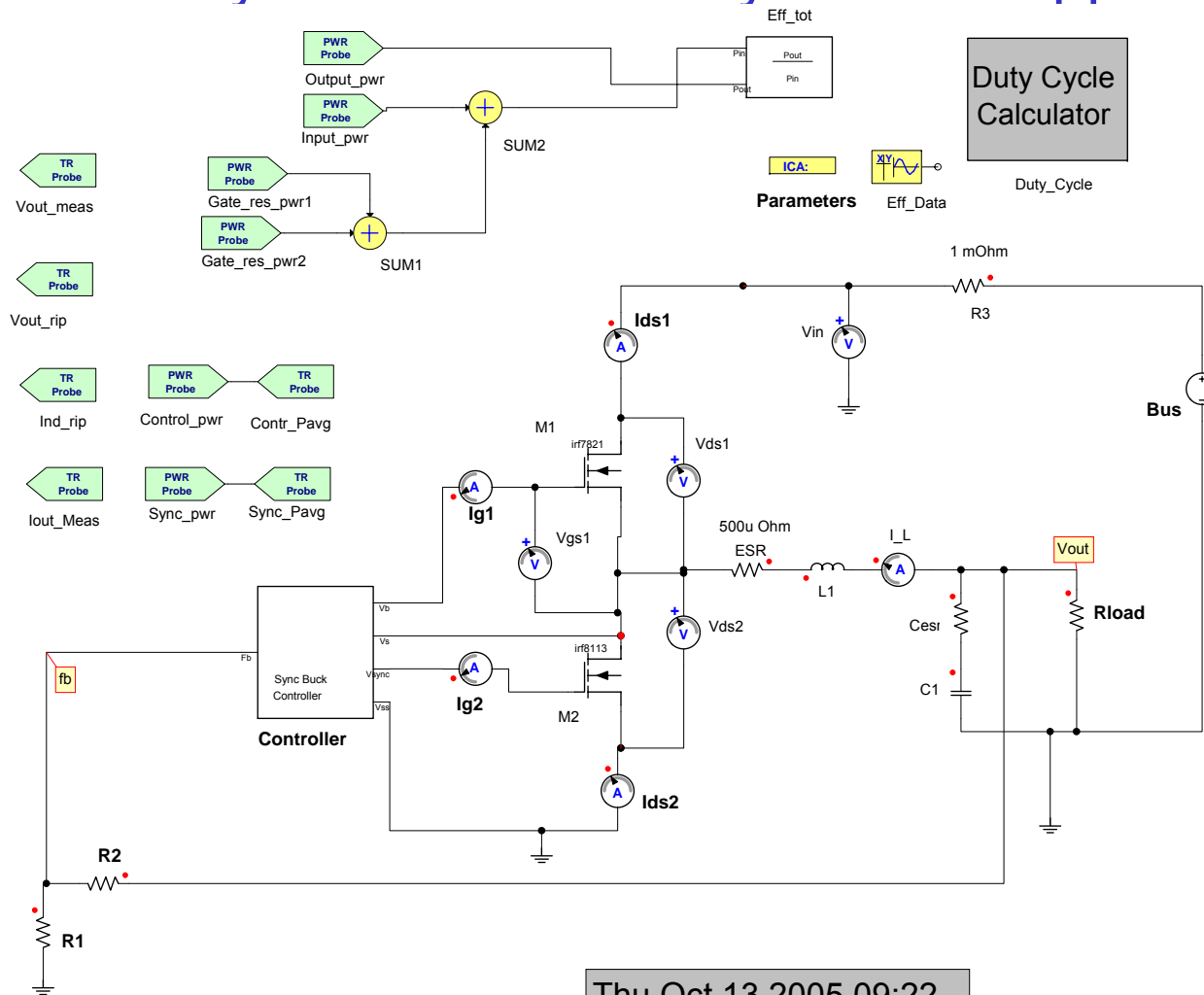
Circuit Parameters



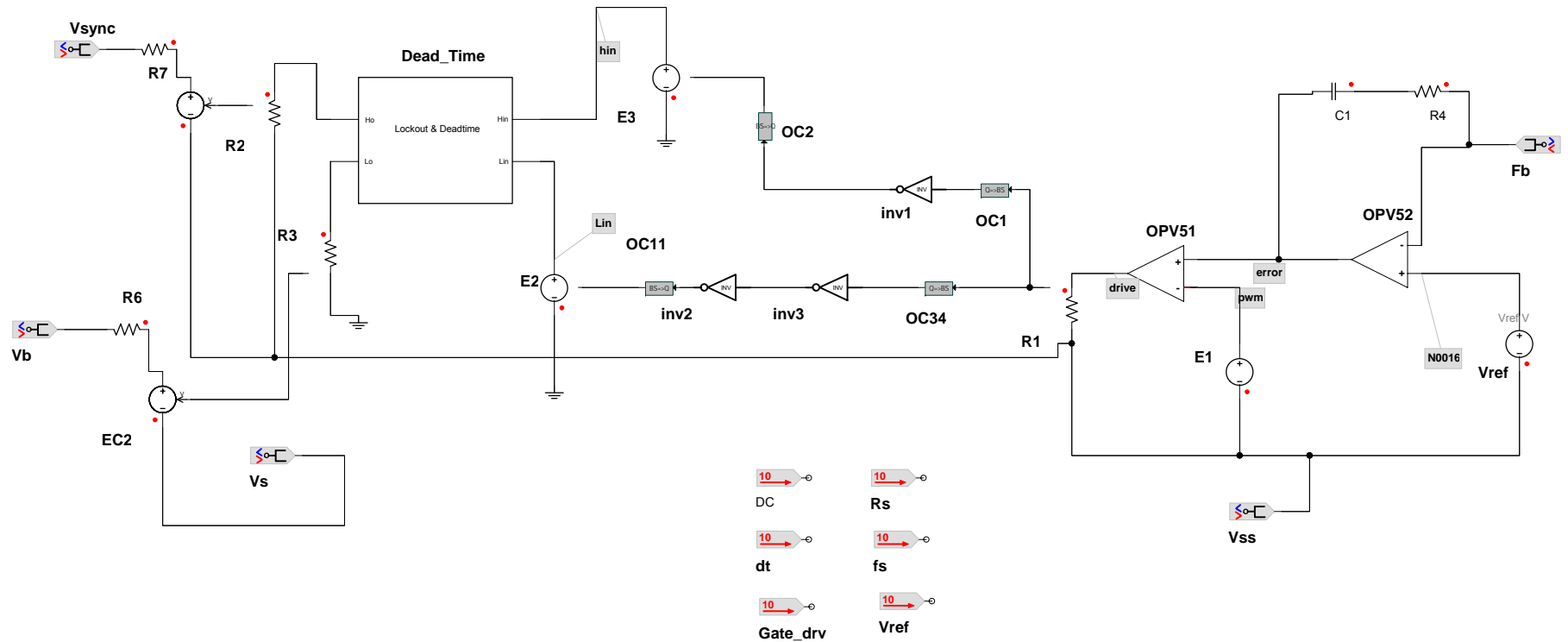
Input Parameters

Calculated Circuit Parameters

Steady State Model of Sync-Buck Application

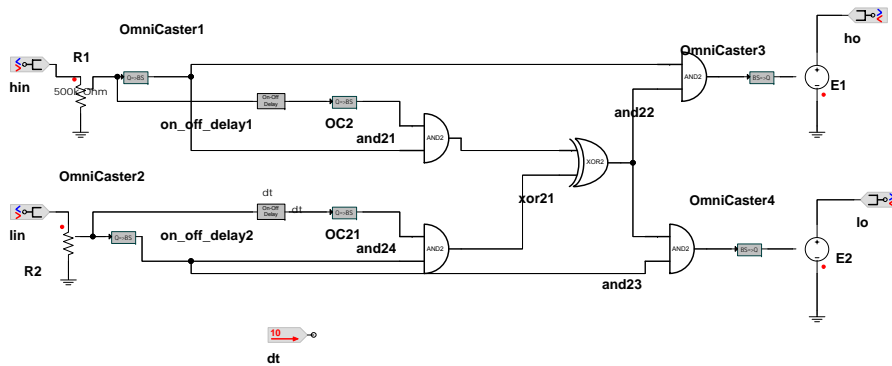


Steady State Model of Sync-Buck Application

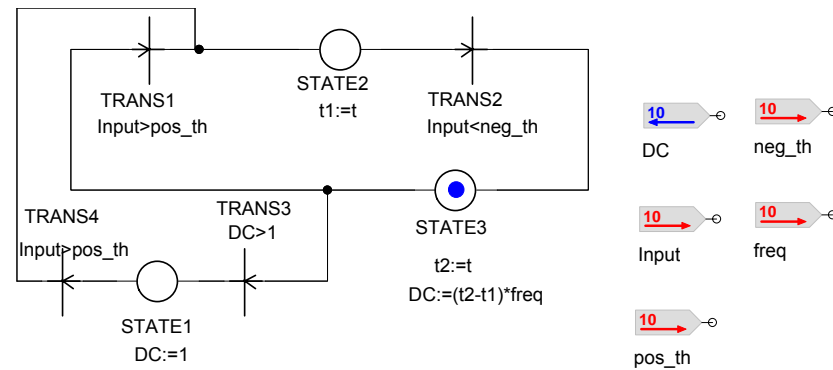
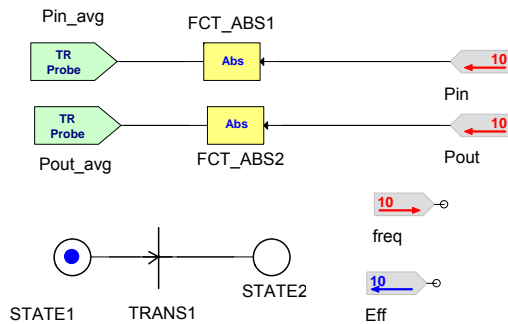


Controller Model

Supporting Models



Dead Time Model



"Duty Cycle Skipping (No transition in period) DC set to 1"

Duty Cycle Calculation Model

Efficiency Calculation Model

Steady State Transient Simulation Results

Input Parameters	
Name	Value
Vin	12.00
R1	1.00k
iload	10.00
fs	400.00k
Vout	1.80
dI	150.00m
Vout_rip	50.00m
Vref	800.00m



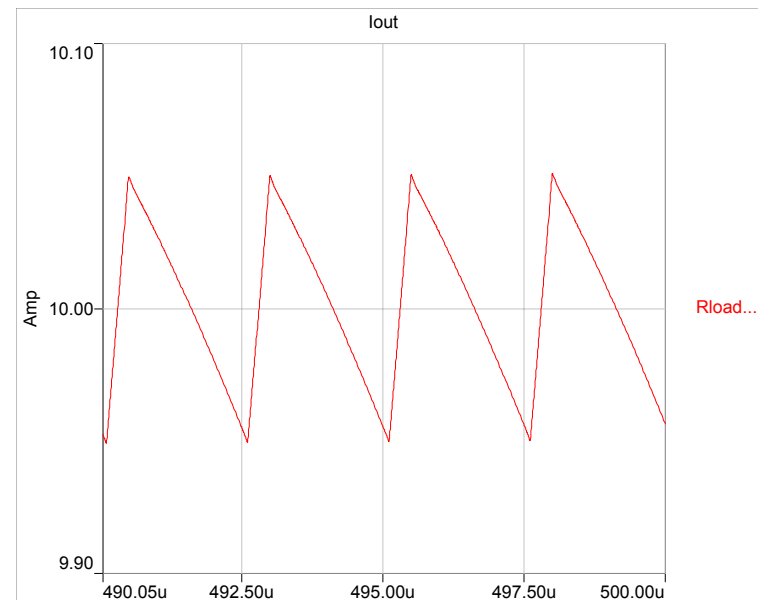
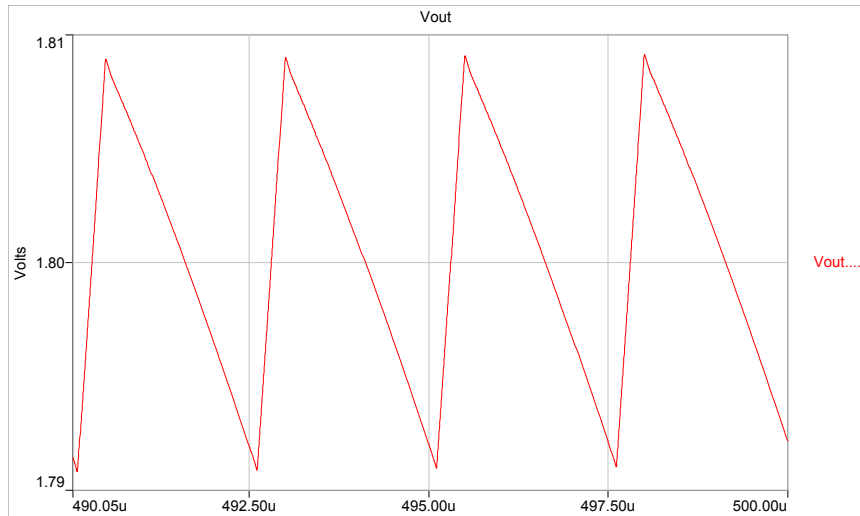
Calculated Parameters	
Name	Value
DC	150.00m
R2	1.25k
rload	180.00m
L	25.50u
C	7.50u
Cesr	333.33m



Measured Parameters	
Name	Value
Vout_rip.PKPK	18.40m
Vout_meas.MEAN	1.80
Ind_rip.PKPK	156.29m
Iout_Meas.MEAN	10.00
Contr_Pavg.MEAN	1.15
Sync_Pavg.MEAN	2.05
Duty_Cycle.DC	148.40m
Eff_tot.Eff	81.54
Eff_meas	82.96

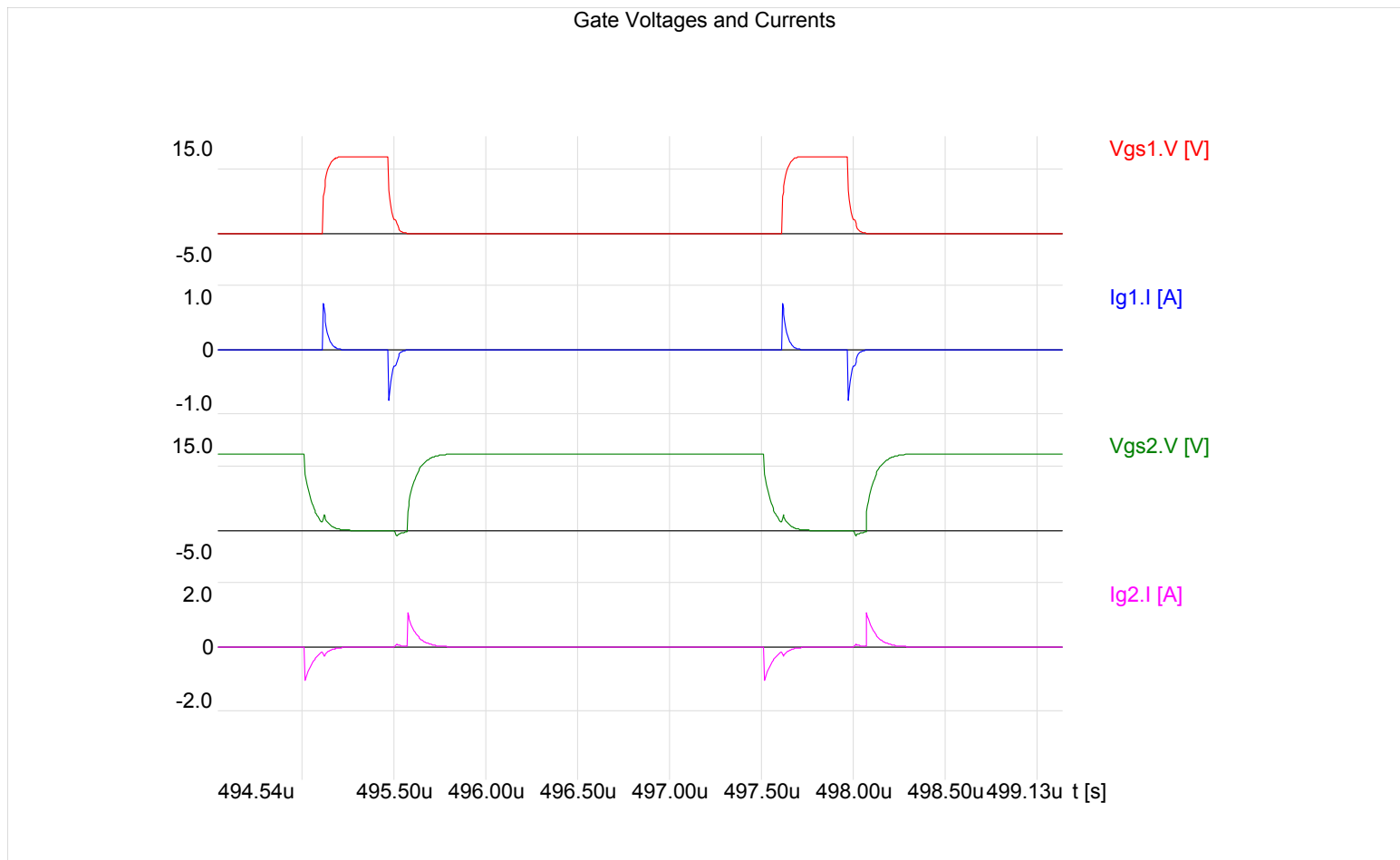
Results from a 500uS transient run

Steady State Transient Simulation Results

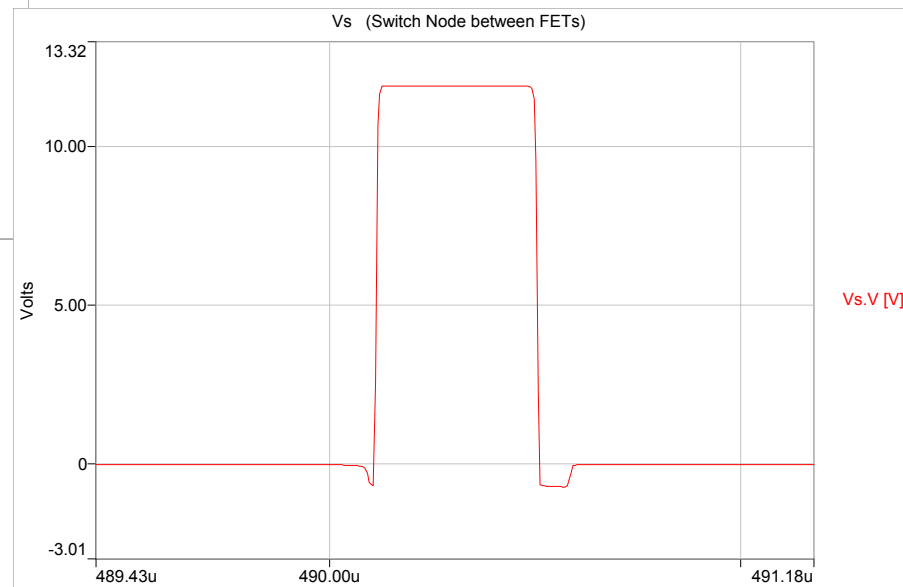
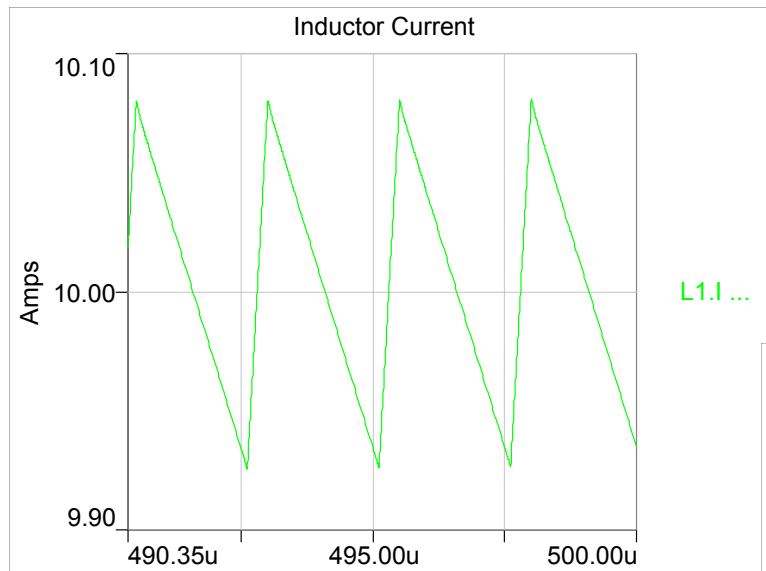


Converter Output Voltage & Current

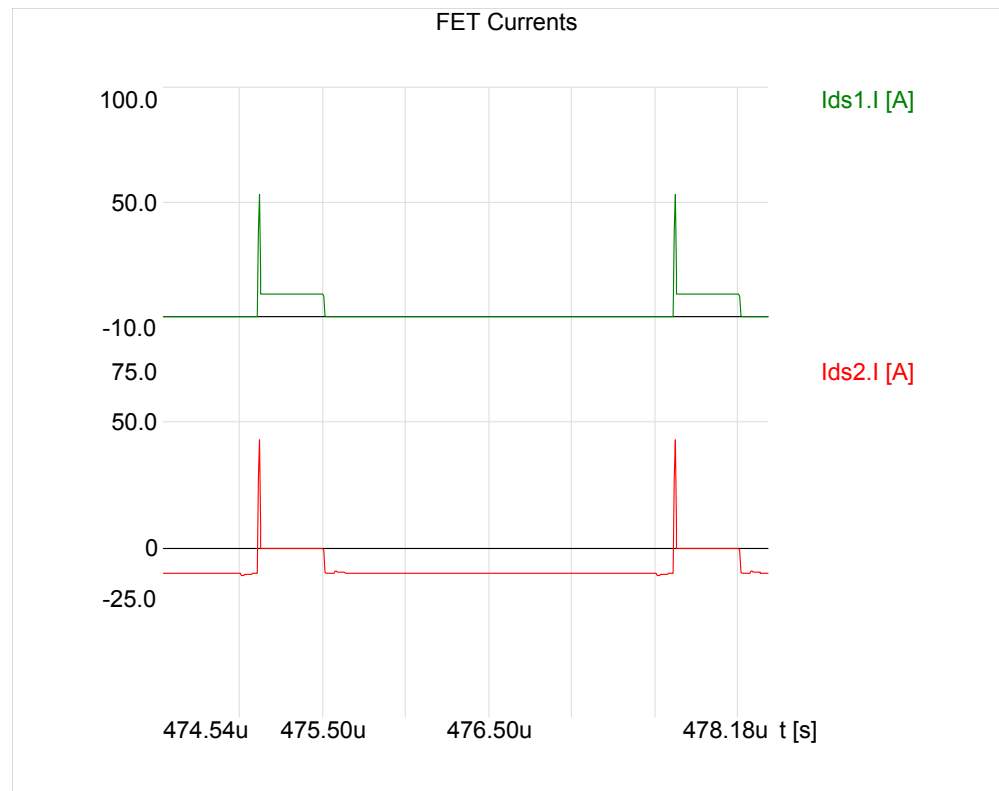
Steady State Transient Simulation Results



Steady State Transient Simulation Results

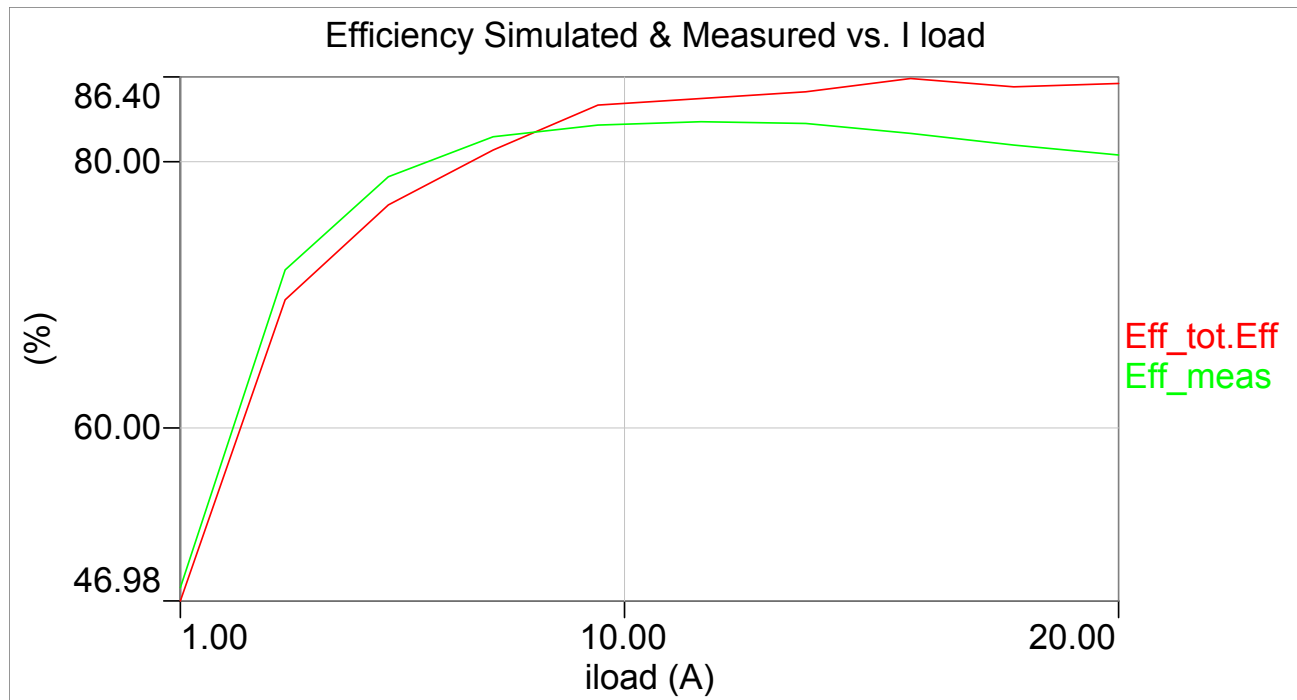


Steady State Transient Simulation Results



Body Diode Reverse Recovery is illustrated by the spikes.

Efficiency Curve



Output current swept from 1A to 20A to give Efficiency (%) vs. Output Current.

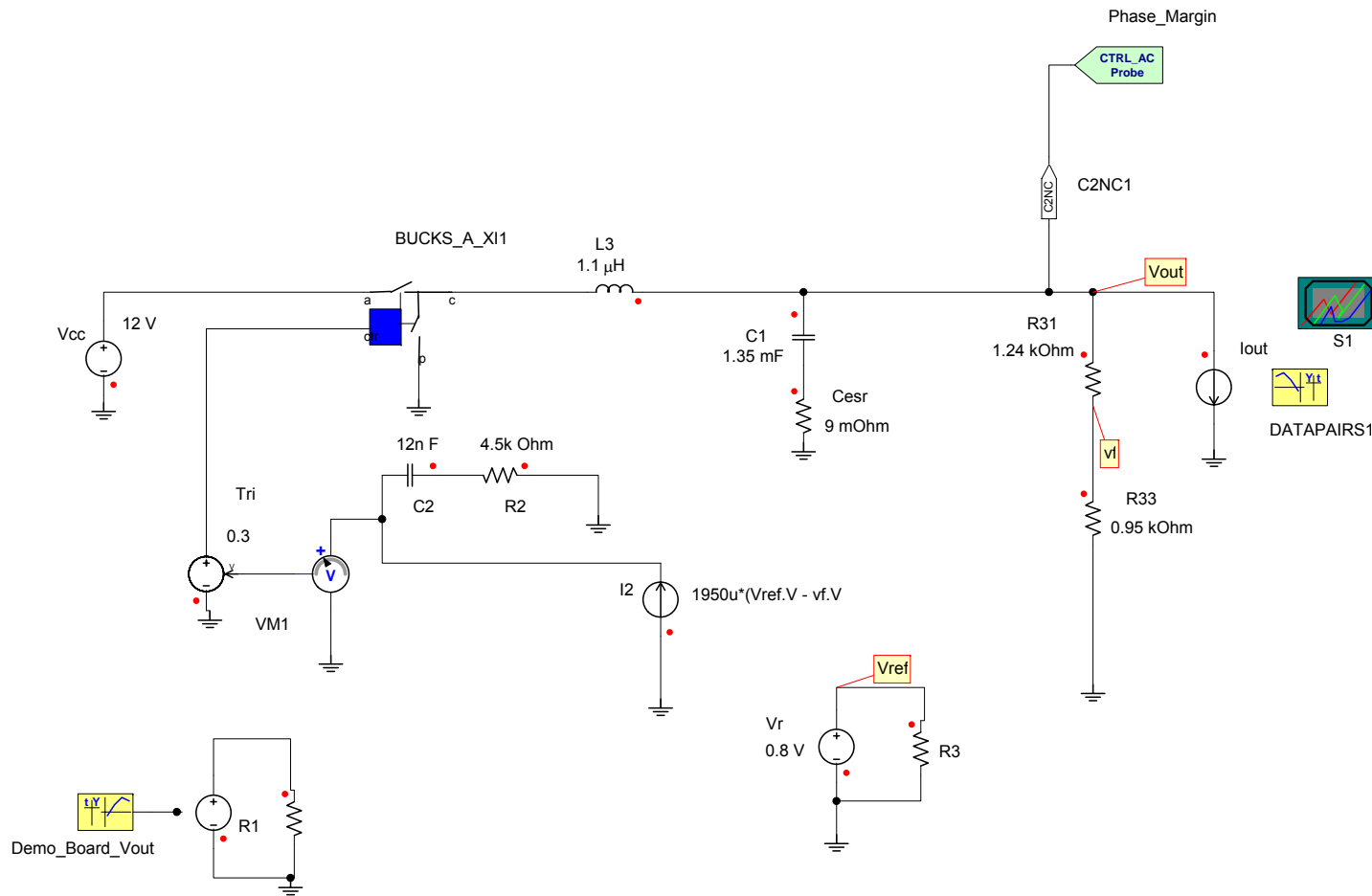
Eff_tot.Eff – Simulation

Eff_meas – From IR3621 demo board measurements

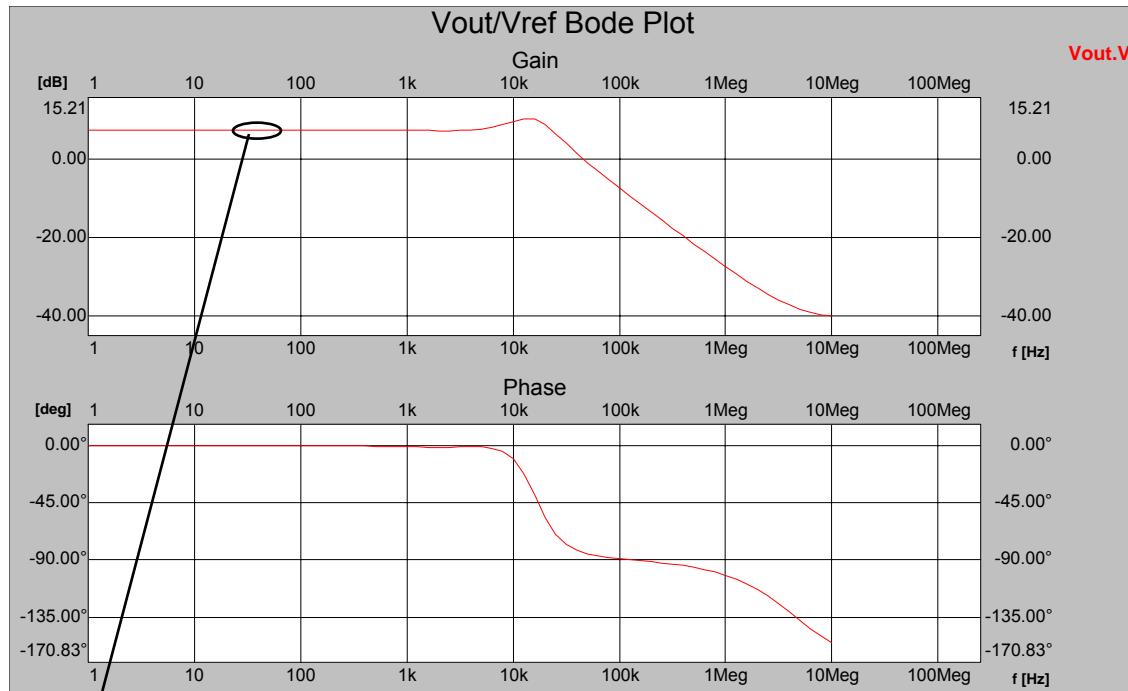
AC and Transient Response Analysis of Circuit

- **Purpose**
 - Circuit stability criteria analysis (Phase Margin)
 - Evaluate transient response
- **Limitations**
 - Trade-off fast simulation time for lost of switching waveform information.
 - Can't evaluate PWM switch effects on transient response.

State Average Model Schematic



Bode Plot and Phase Margin



7.25db=> gain of 2.304
 $V_{ref}=0.8V$ $V_{out}=1.84V=2.304*0.8V$

Phase Margin

Name	Value
Phase_Margin.PM (real) [deg]	96.05

Statistical Analysis of Phase Margin

Properties - PM_Monte

Task Properties | Parameter | Performance Measurement

St...	Name	I...	Value Distribution	Boundary Determination	Minim...	Maxim...	Mean Value	Standard Deviation	Tolerance
<input checked="" type="checkbox"/>	L3.L	...	Uniform Distribution	Mean Value & Tolerance	3	5	1.1u	6.66666666666667	20
<input checked="" type="checkbox"/>	R31.R	...	Uniform Distribution	Mean Value & Tolerance	3	5	1.25k	666.66666666666...	2
<input checked="" type="checkbox"/>	R33.R	...	Uniform Distribution	Mean Value & Tolerance	3	5	1k	666.66666666666...	2
<input checked="" type="checkbox"/>	Cesr.R	...	Uniform Distribution	Mean Value & Tolerance	3	5	9m	6.66666666666667	20
<input checked="" type="checkbox"/>	C2.C	...	Uniform Distribution	Mean Value & Tolerance	3	5	12n	6.66666666666667	20
<input checked="" type="checkbox"/>	R2.R	...	Uniform Distribution	Mean Value & Tolerance	3	5	4.5k	1.66666666666667	5
<input checked="" type="checkbox"/>	Vr.EMF	...	Uniform Distribution	Mean Value & Tolerance	3	5	800m	1.66666666666667	5
<input checked="" type="checkbox"/>	Vcc.EMF	...	Uniform Distribution	Mean Value & Tolerance	3	5	12	1.66666666666667	5

Adjust Parameter

Value Distribution: Uniform Distribution

Boundary Determination:

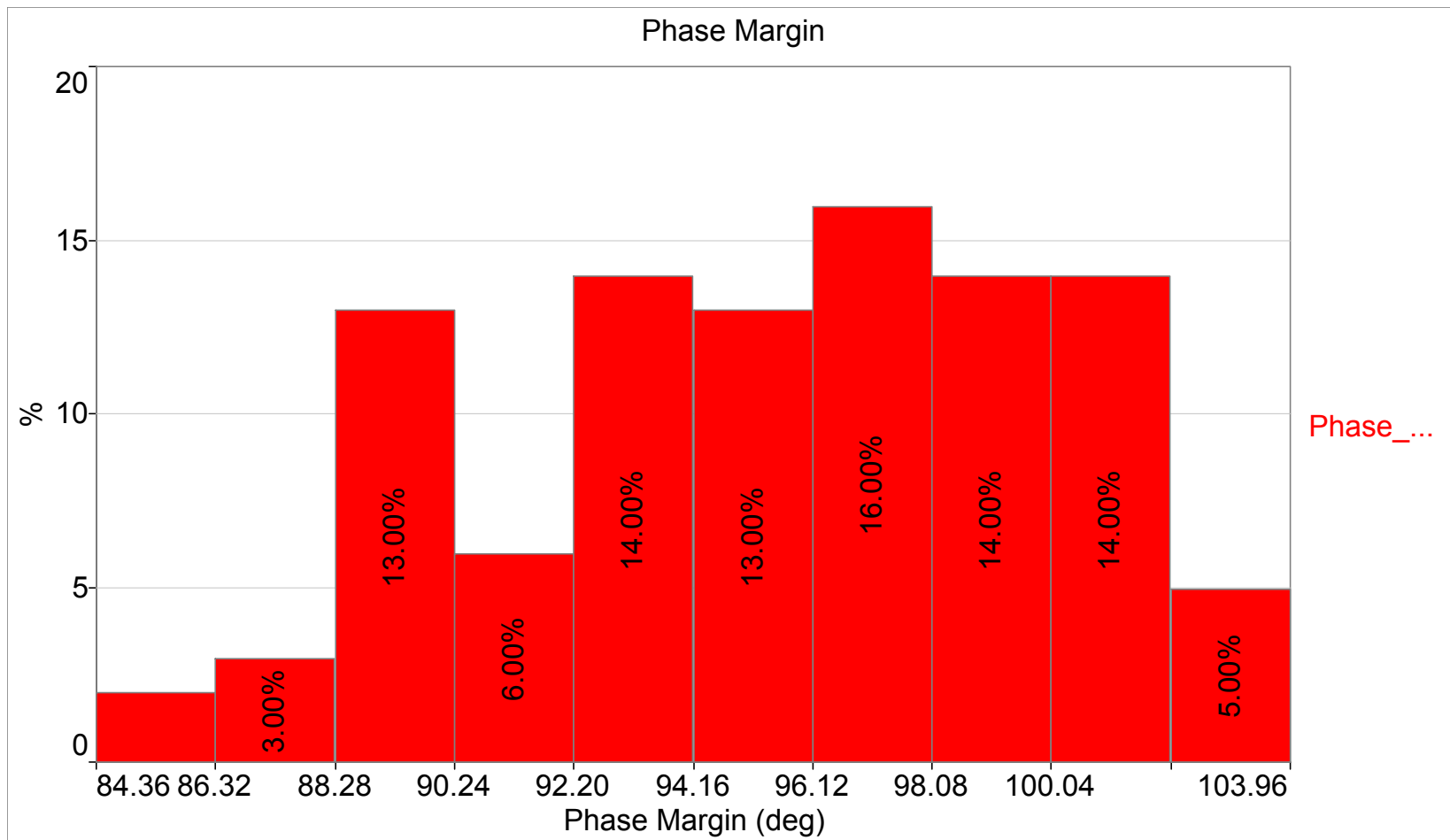
Minimum:

Standard Deviation:

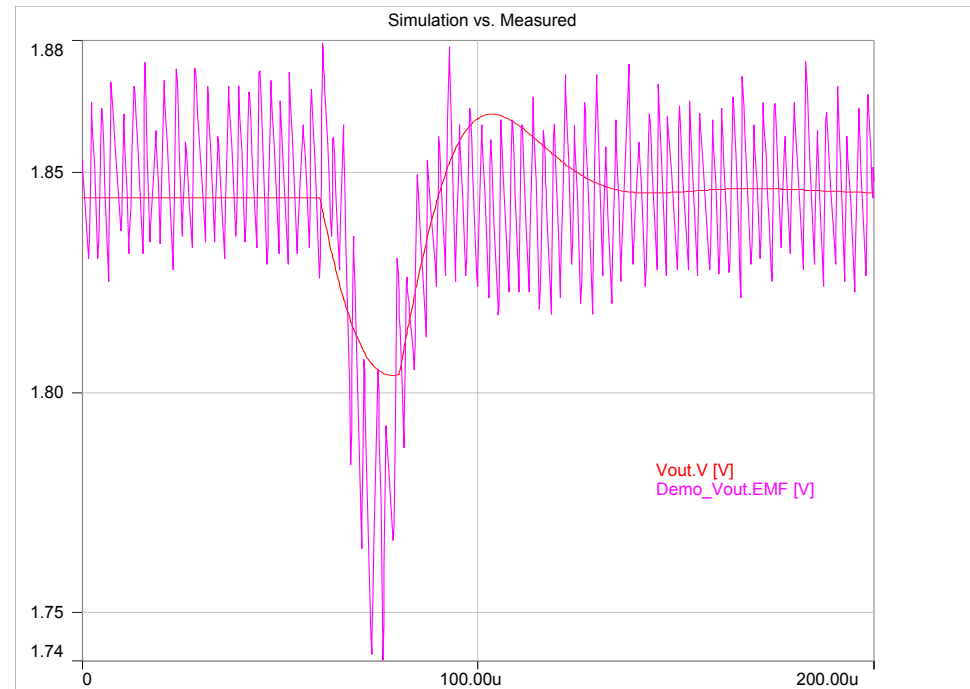
Tolerance:

OK Cancel Apply Help

Monte Carlo Results for Phase Margin



10A Load Step



A 0A to 10A load step was simulated in order to demonstrate the step response of the system.

Vout.V [V] – Simulation

Demo_Vout.EMF [V] – IR3621 Demo board measurement

Conclusion

- **Using vendor spice models and non-language based modeling techniques, a sync buck design can be thoroughly analyzed before commitment is made to hardware.**
- **PWM model is used to evaluate power dissipation, efficiency, and the various signals in the circuit in steady state.**
- **Use of PWM model yields slow simulation times (~2min/run)**
- **State average model is used to evaluate circuit stability and circuit transient response.**
- **Use of State average model yields fast simulation times (<1 second/run)**
- **Results can be compared to hardware measurements.**