ANSOFT CORPORATION PRESENTS:

CONVERGE

AN APPLICATIONS WORKSHOP FOR HIGH-PERFORMANCE DESIGN

Design of De-Emphasis and Equalization Circuits for Gigabit Serial Interconnects

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Agenda

- High Speed Interconnects
  - Driving forces
  - Challenges
- Equalization Techniques
- De-emphasis Circuitry compliant with FB-DIMM standard
  - Circuit schematics
  - Nexxim Simulation Results
- Example of Passive Equalization at Receive side
- Example of combination of transmit and receive equalization

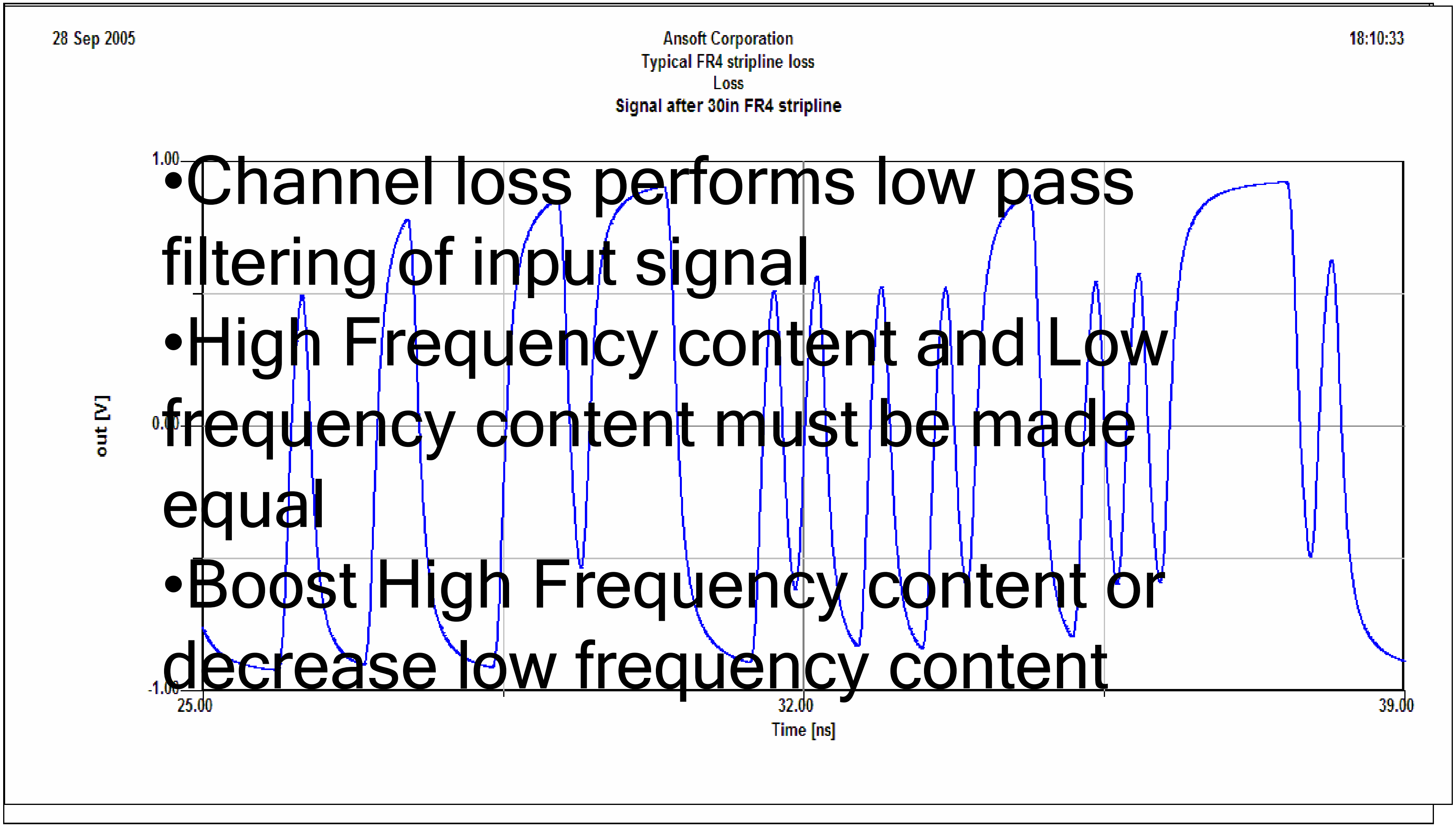
Why High Speed Serial Interconnects ?

- Modern systems like servers, storage, PCs, telecom systems have necessitated large volume of data transmission
- Shared parallel buses get denser and board design becomes complicated and costly
- Solution is to move to gigabit serial links with more complicated IC design since Silicon manufacturing cost is shrinking

Challenges of High Speed Serial Transmission

- Signal Integrity
  - Channel Loss hampers board design
    - Skin Loss $\propto \sqrt{(freq)}$
    - Dielectric Loss $\propto$ freq
  - Impedance Mismatch
  - Lossy Connectors
- Verification and testing of high speed designs
  - Inaccurate modeling and simulation of channel, vias, interconnect
  - Accurate transistor models
- New Simulation Tools and Diagnostics

FR4 loss



- Channel loss performs low pass filtering of input signal
- High Frequency content and Low frequency content must be made equal
- Boost High Frequency content or decrease low frequency content

Potential Solutions

Equalization must be employed to deal with channel loss

- Transmit Equalization
  - Pre-Emphasis: Increase in voltage swing for transition bits (Boost High Frequency content)
  - De-Emphasis: Reduce voltage swing for non-transition bits (Attenuate Low Frequency content)
- Receive Equalization
  - Analog Techniques: High Pass Filter to reverse channel effect
  - Digital Techniques: Decision Feedback Equalization

Transmit vs. Receive Equalization

- Which method to adopt?
  - Pre-Emphasis/De-Emphasis used if noise is a big factor, receive equalization amplifies transmitted noise
  - Receive Equalization used if cross talk/radiated emissions is a factor
  - Receive Equalization can be implemented with a passive network without a system clock
- Many systems adopt a combination of the two schemes

FB-DIMM Standard

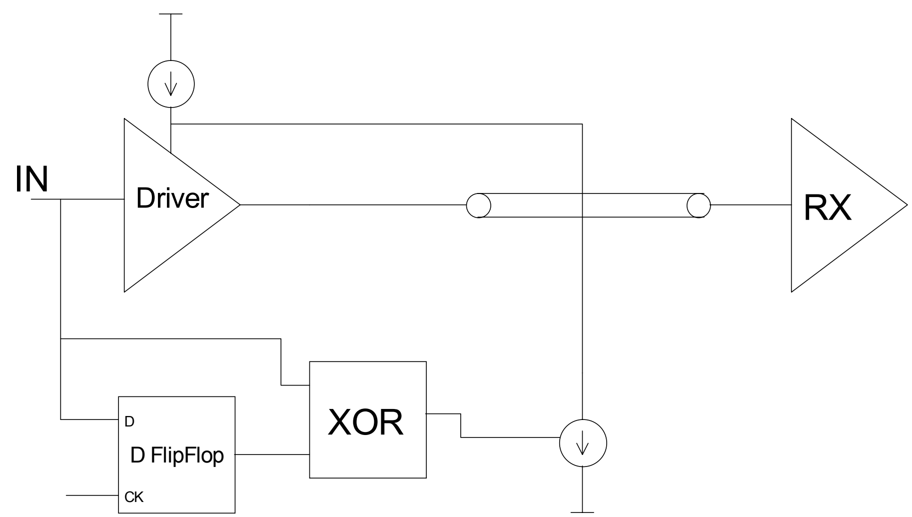
Signaling Features

- DC coupled output
- Transmitter with de-emphasis (3.5dB & 6dB)
- Reference clock at 1/24 of data rate
- Data transmission at 3.2 Gb/s, 4.0 Gb/s and 4.8 Gb/s
- 50 Ω single ended termination

De-Emphasis Architecture

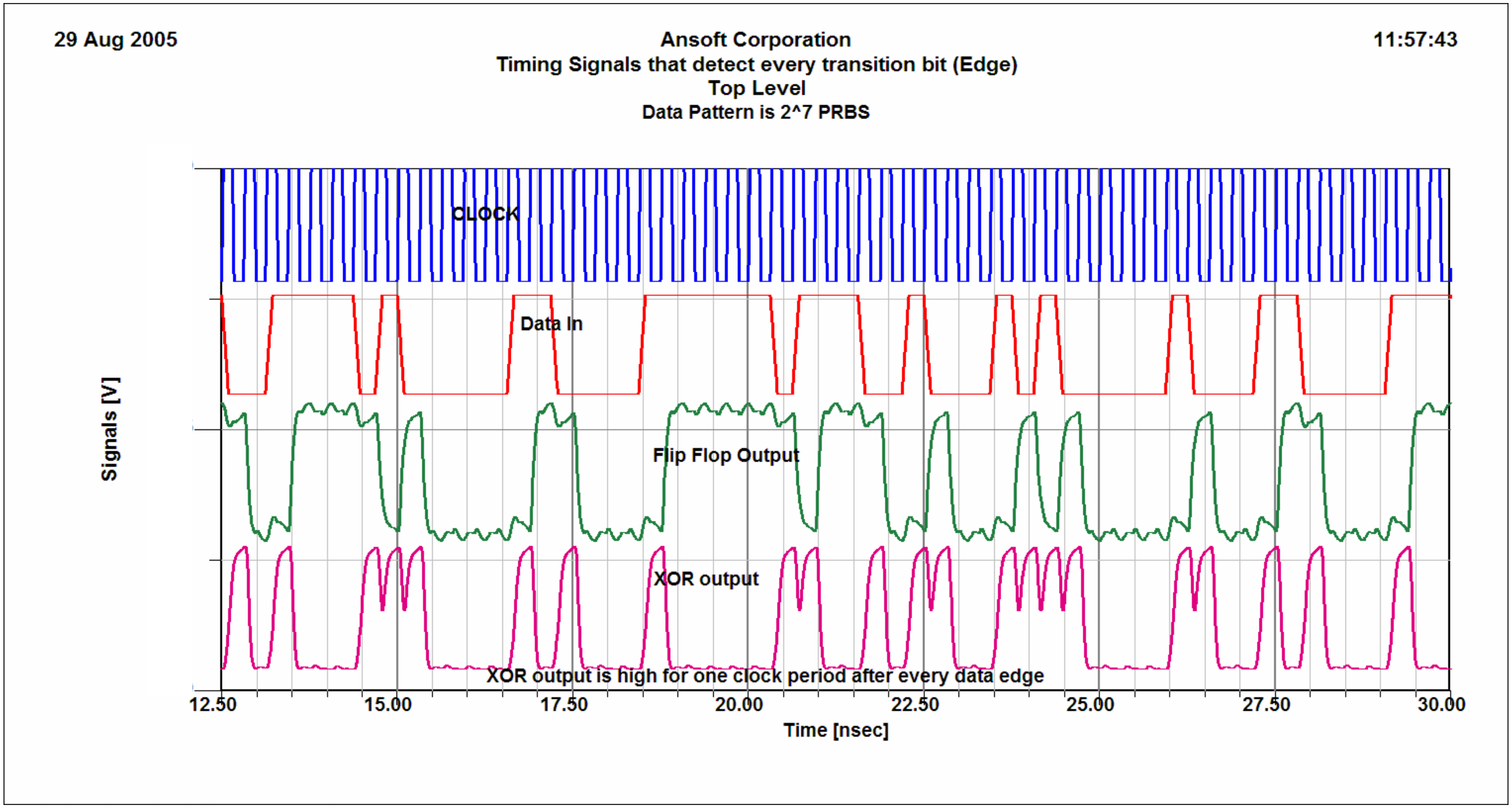
Use edge detection circuitry to detect transition bits

- Delay data by one clock cycle using a positive edge triggered flip-flop.
- XOR data with flip-flop output to generate a pulse (width=clock period) for every transition.
- Use this pulse to control a high speed current mirror that changes the tail current of the output driver to reduce voltage of non-transition bits.
- Block level implementation



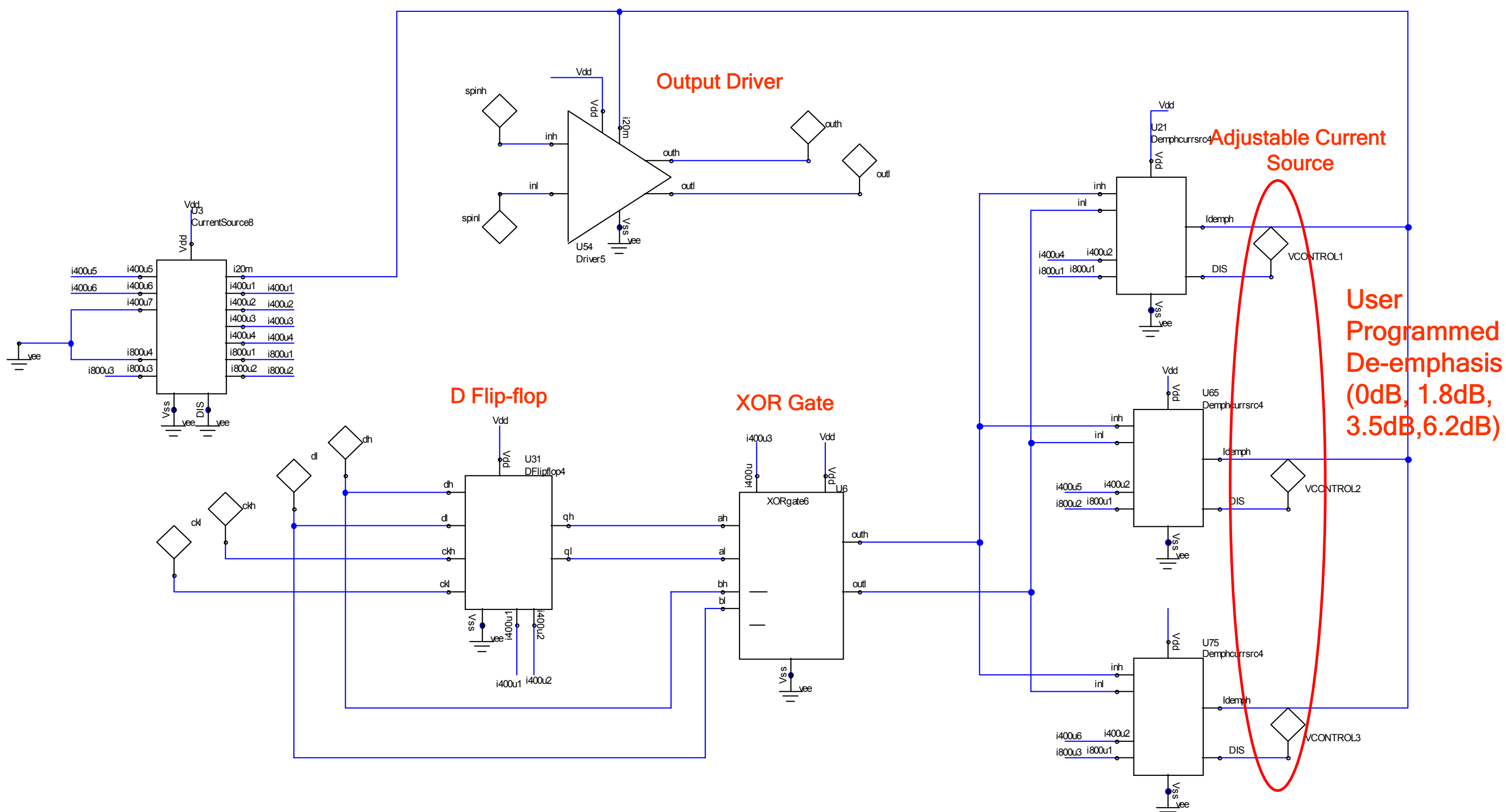
Control Waveforms

- Timing Diagram to show signals that used by the Edge Detection Circuit
- Output of XOR gate is high after every transition



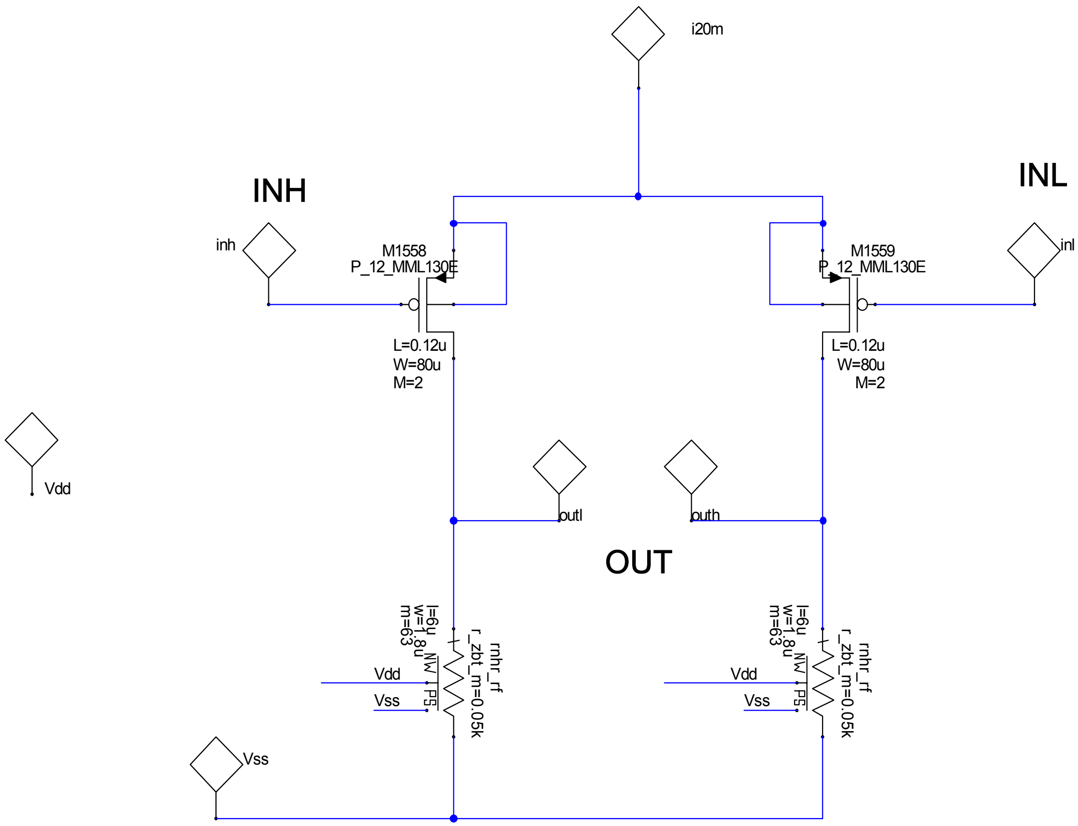
Transmitter Top Level Implementation

- Adjustable De-emphasis through Vcontrol1,2,3 (digital control)
- Four levels of De-emphasis possible 6.5dB, 3.5dB, 1.75 dB and 0dB
- All Circuits realized using UMC's 0.13um CMOS process
- Circuits designed using Ansoft DesignerRF and Nexxim



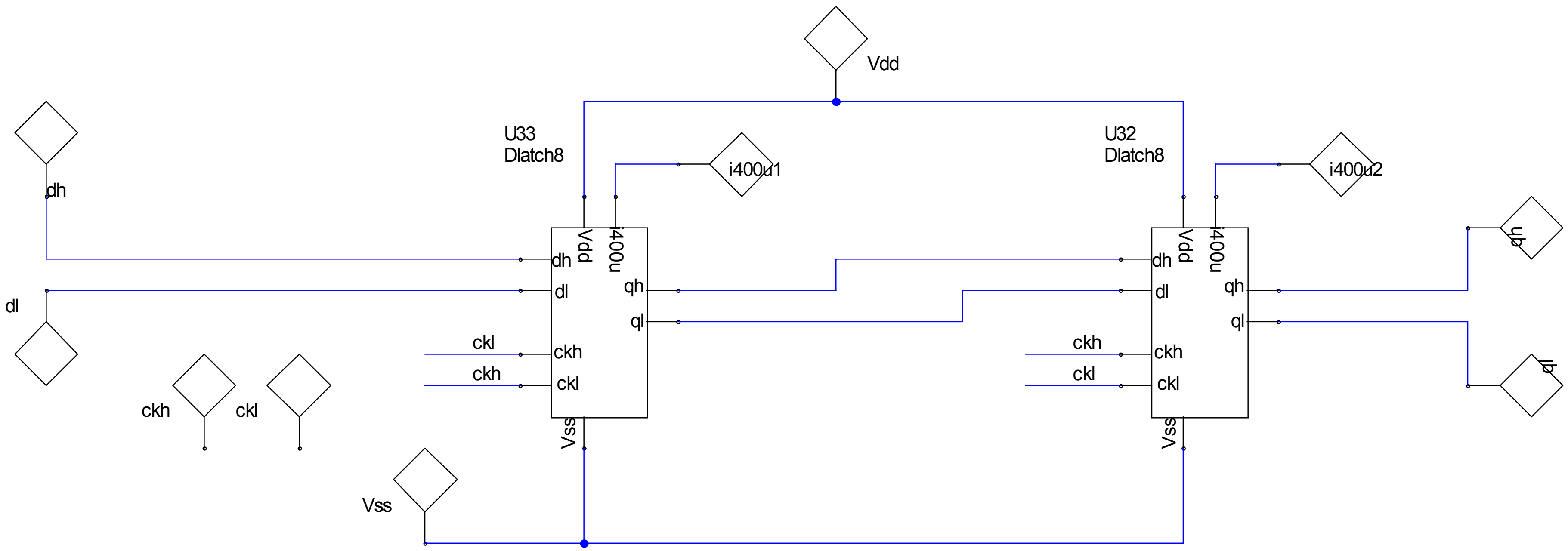
Output Driver

- CML Output Driver
- 50 Ohm load



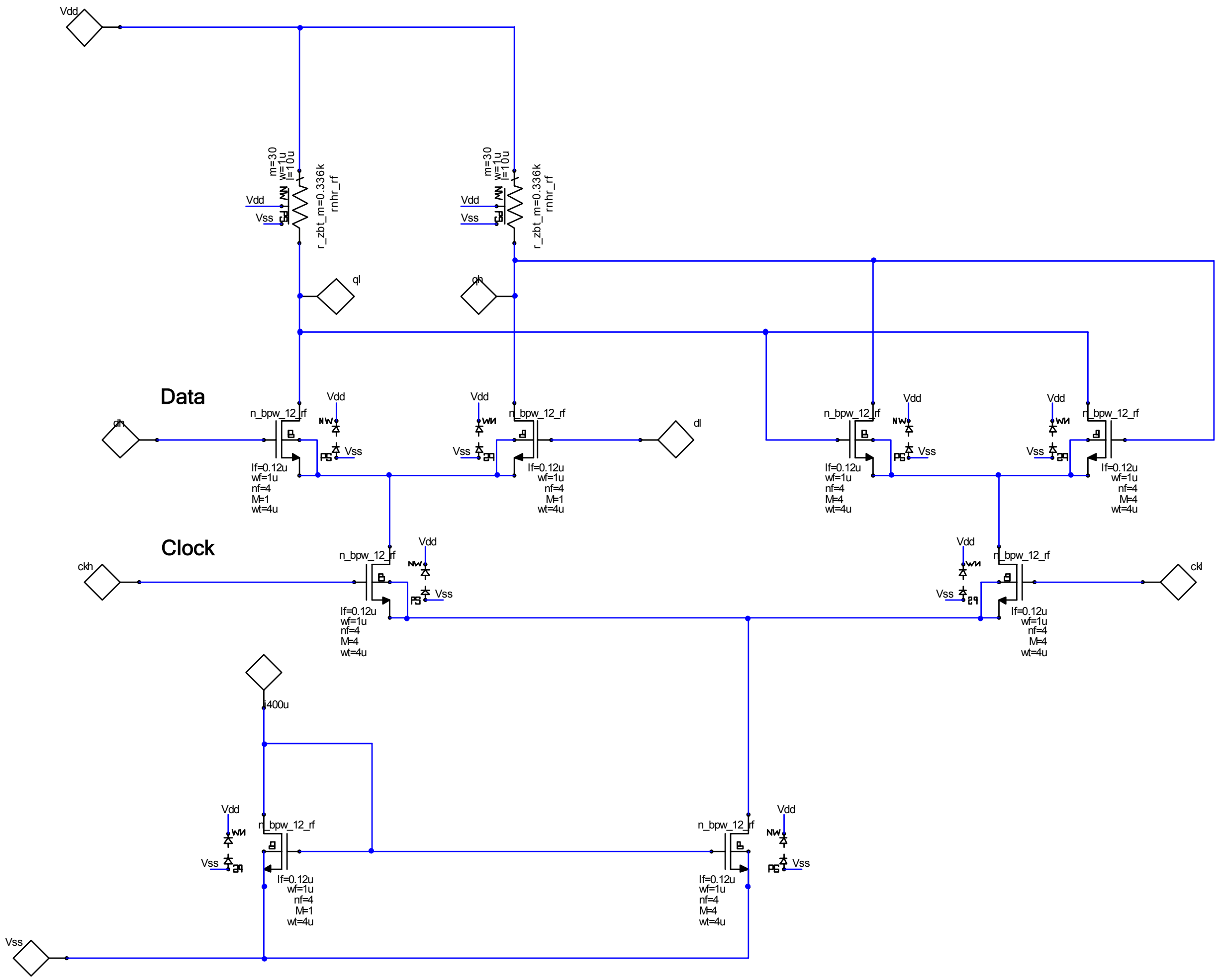
Flip Flop

- D Flip-Flop realized by two D latches in series using complementary clocks
- Optimized for data rates of up to 5Gbps



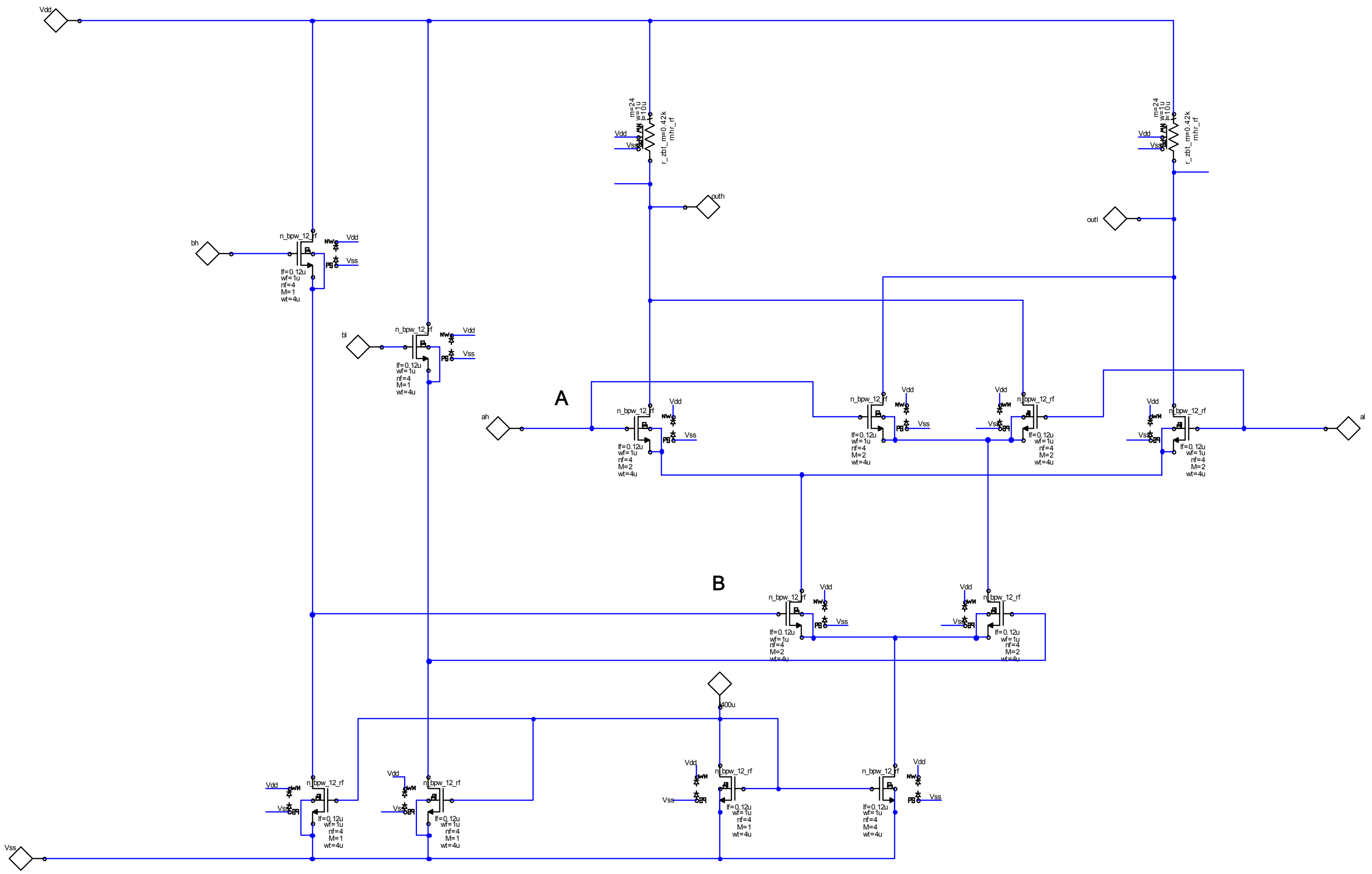
D Latch

- Current Steering D latch with positive feedback



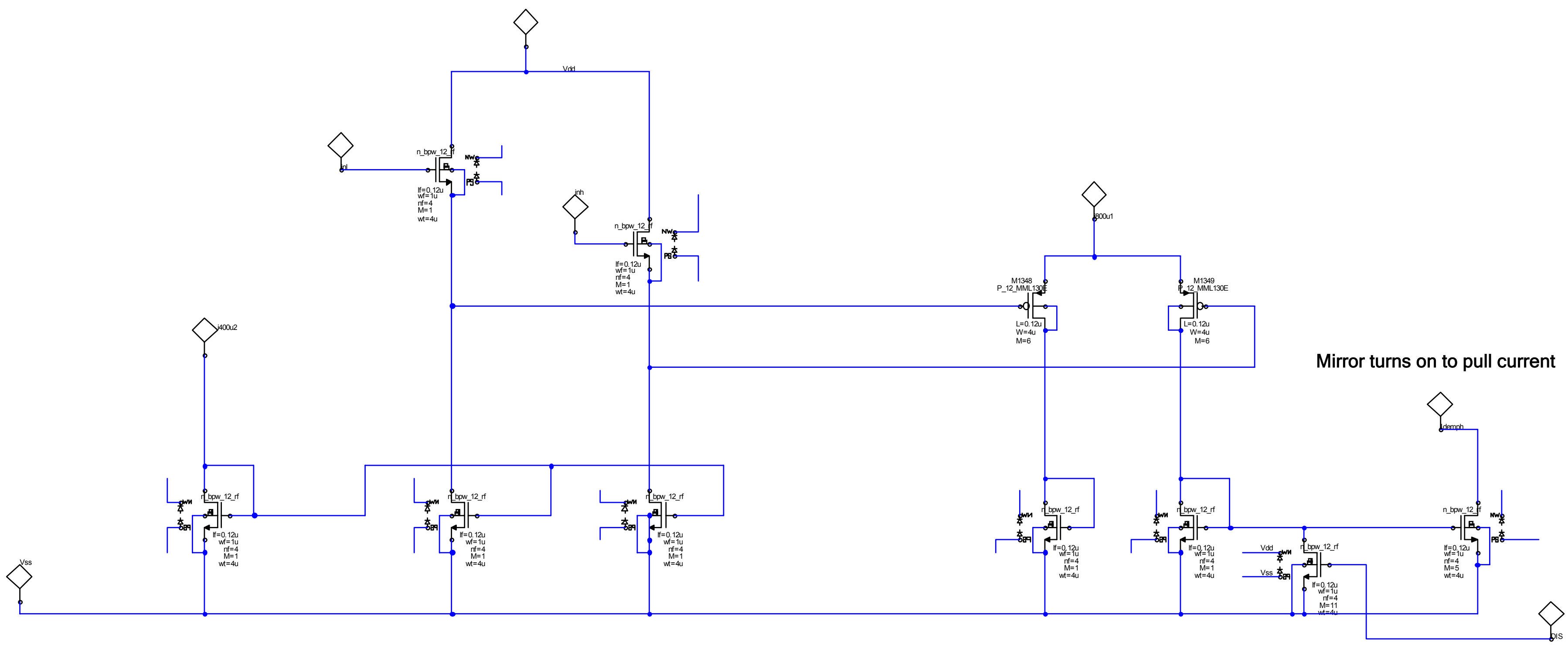
XOR Gate

- Gilbert Cell Variation



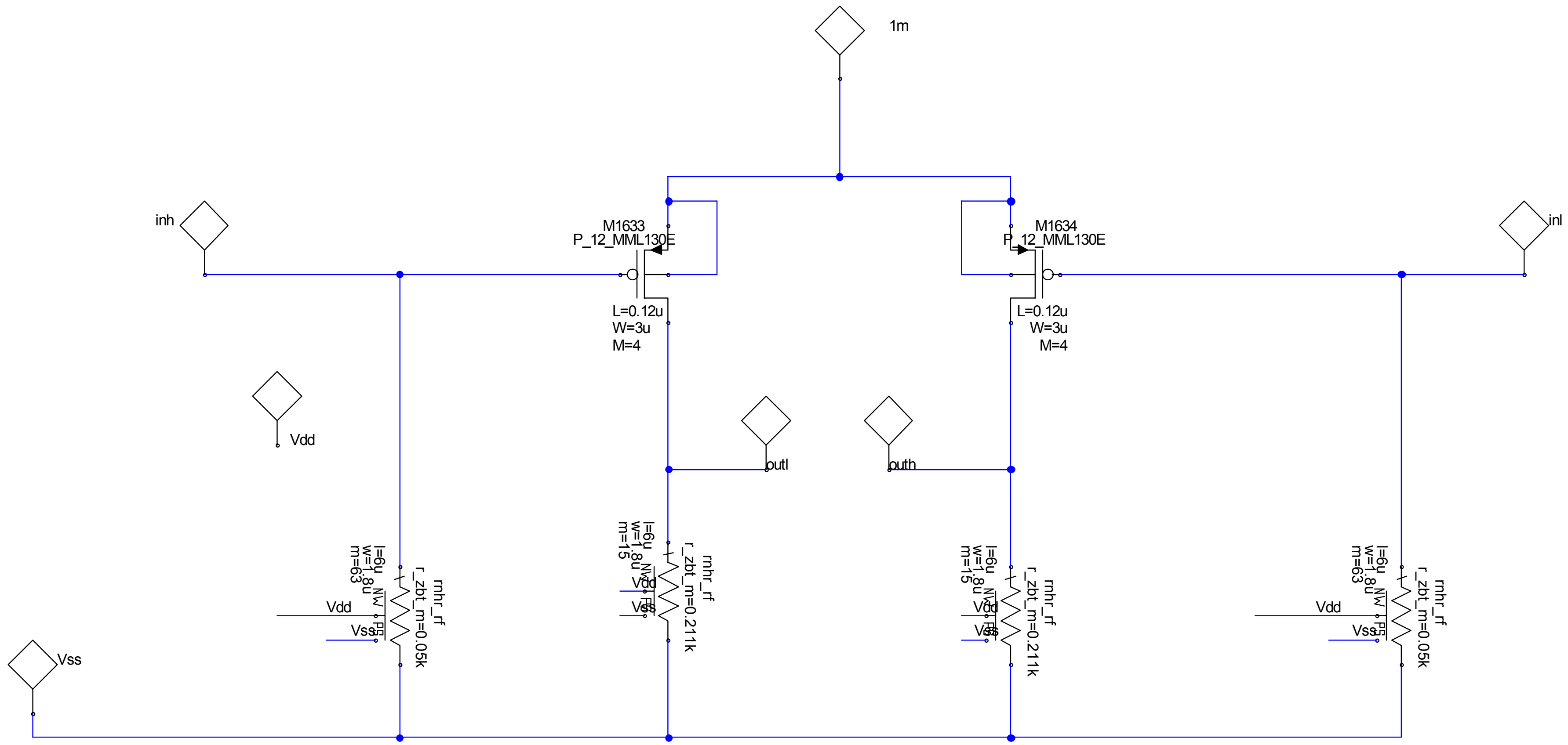
High Speed Current mirror switch

- Changes bias current in driver to incorporate de-emphasis



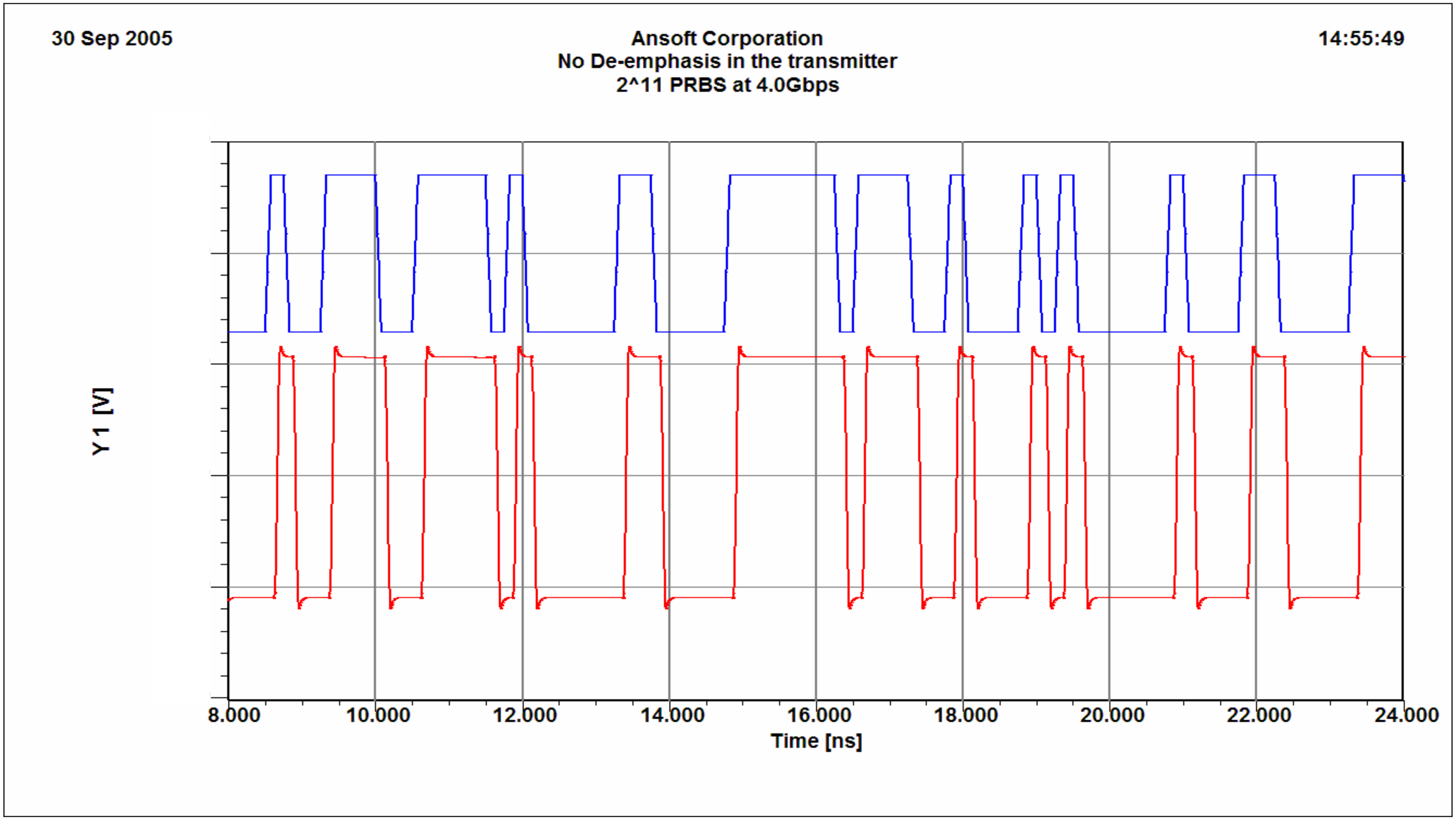
Receiver Input Stage

- CML input stage with internal 50 Ohm resistors



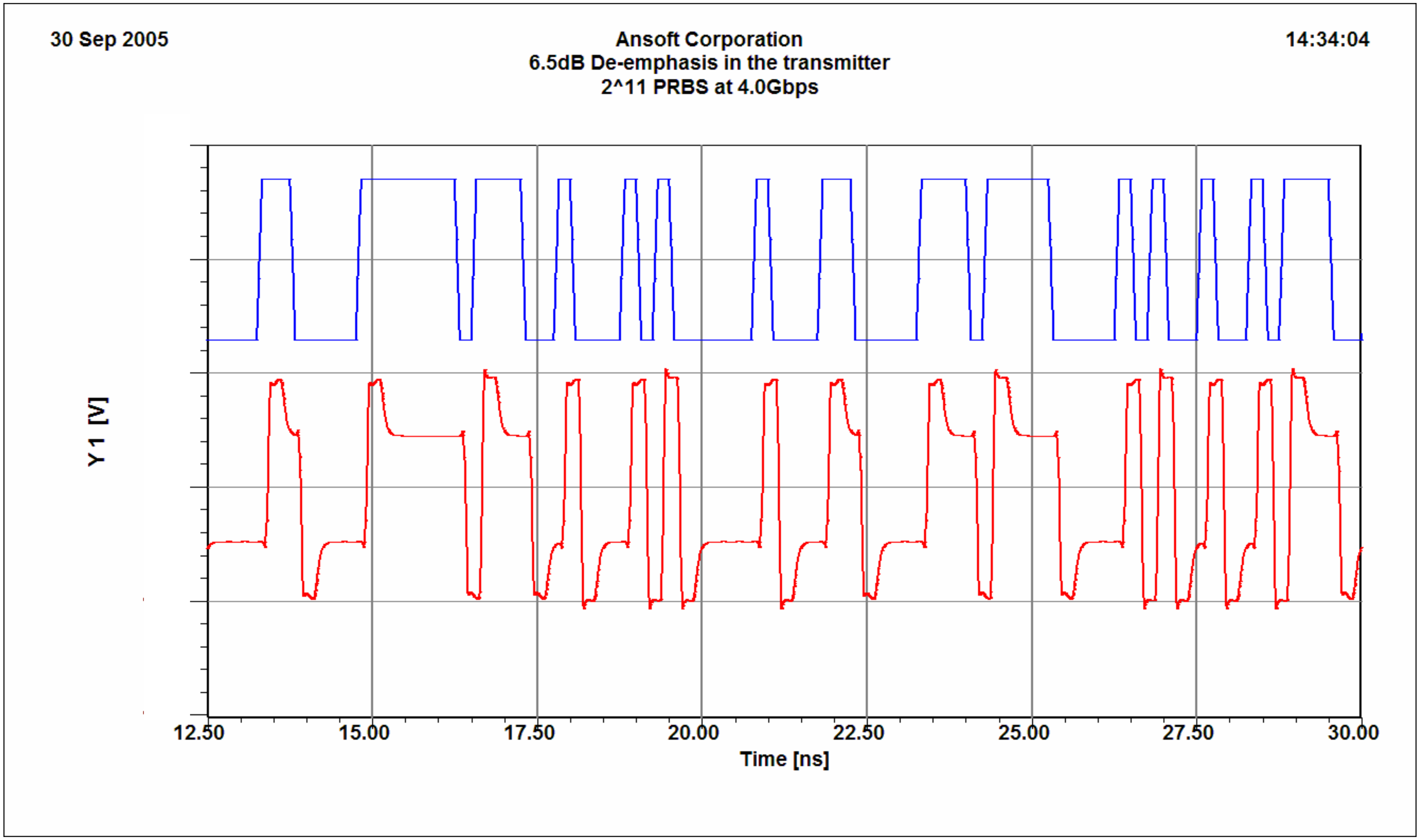
Output without De-emphasis

- De-emphasis disabled

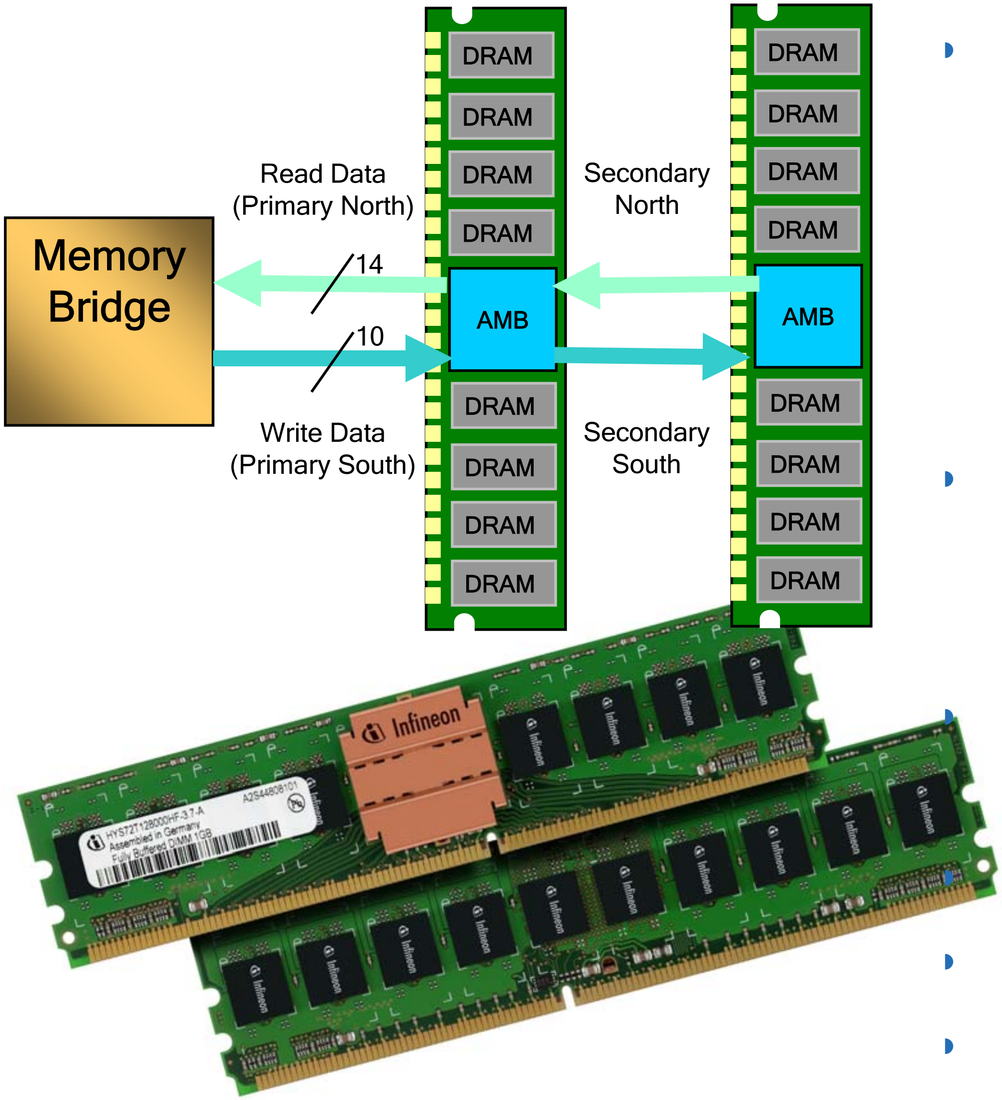


Output with De-emphasis

- Every transition bit is 6.5dB above subsequent bits

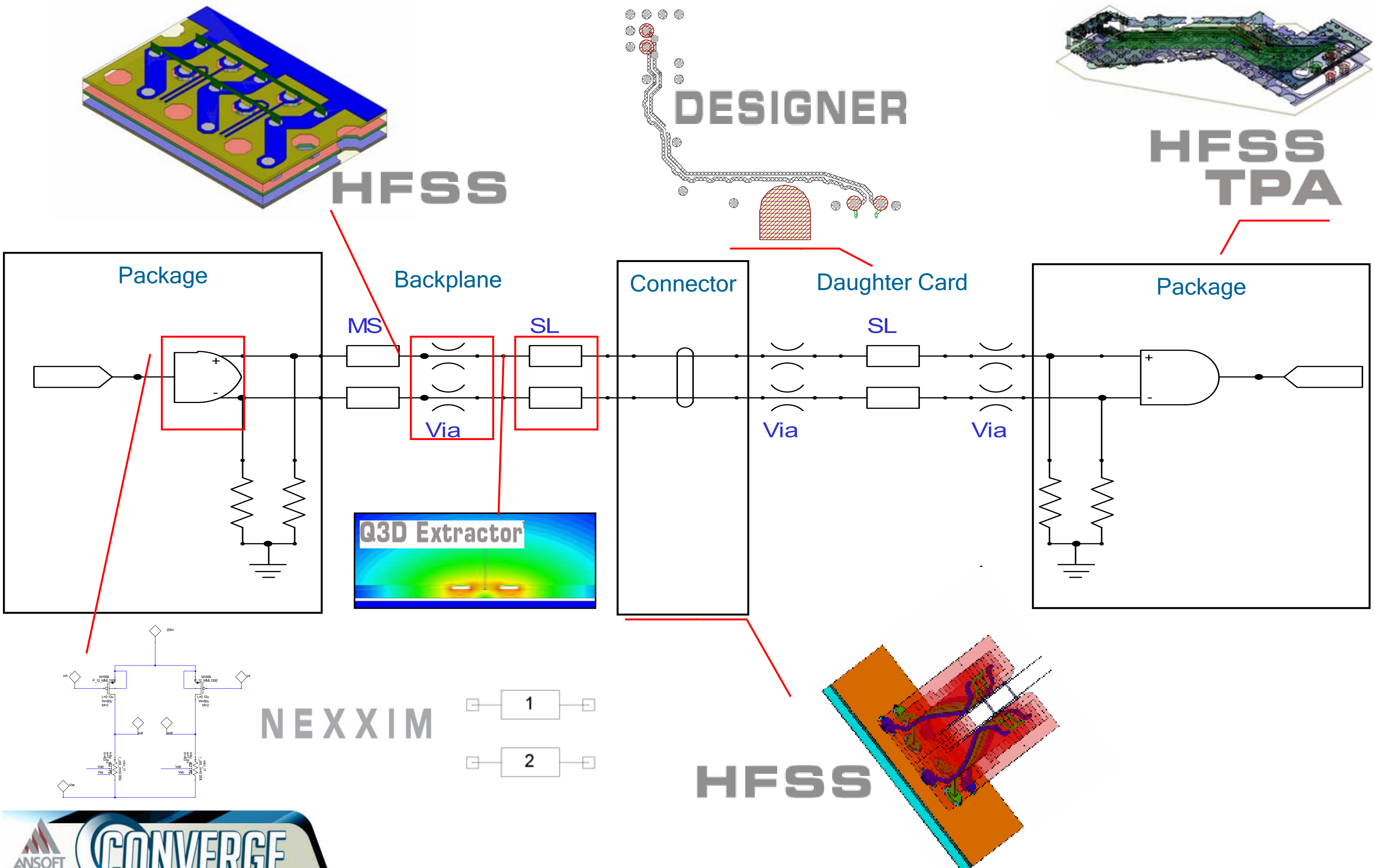


FB-DIMM Configurations



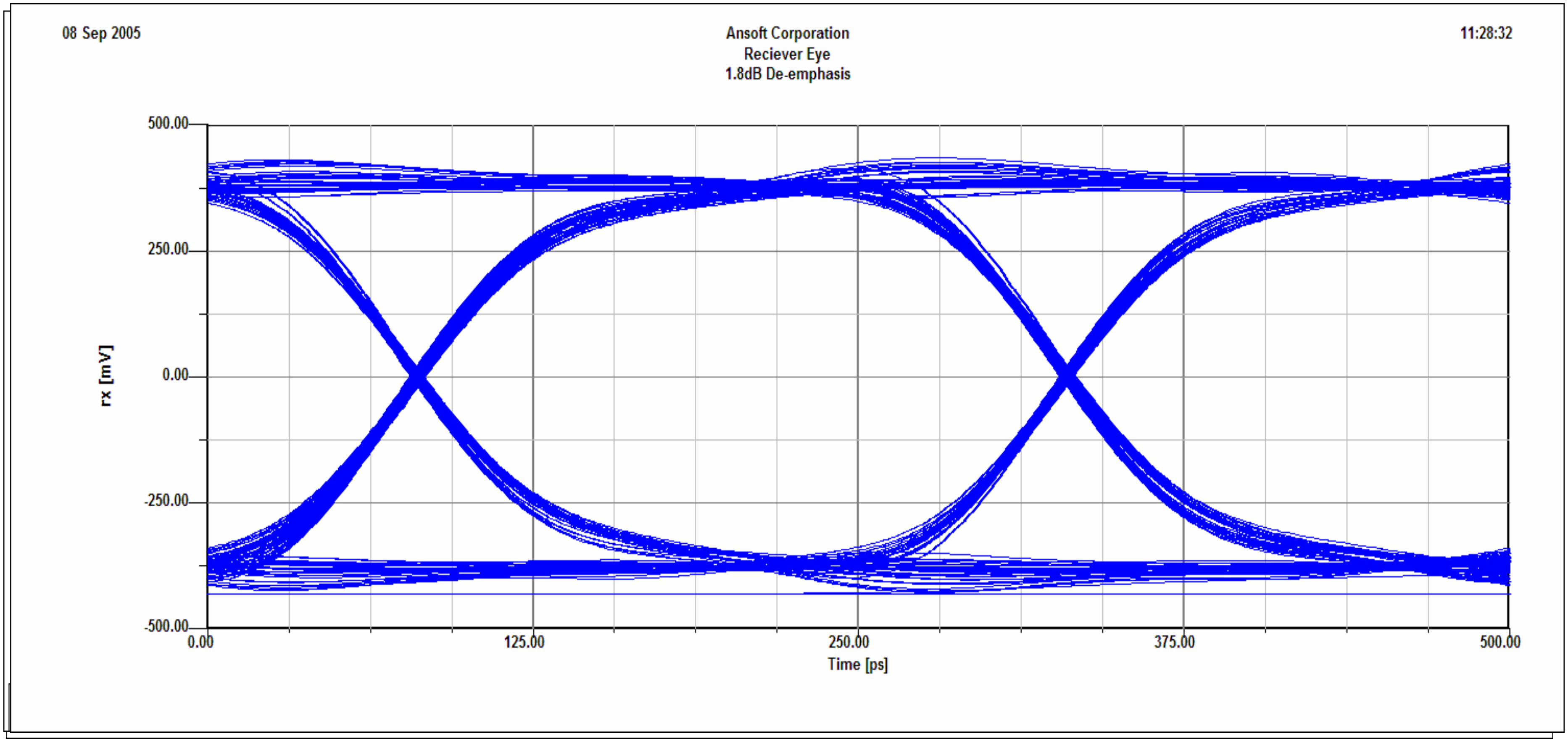
- The FB-DIMM architecture replaces the existing parallel memory bus with a point-to-point serial signaling similar to PCI Express. The DRAM is behind a buffer (Advance Memory Buffer - AMB). The AMB is a high-speed (3.2-5GB/s) unidirectional link with the host memory bridge. Ten channels are provide for writes on the South Bridge and 14 for reads on the North Bridge. The AMB also has a secondary channel for read/writes that acts a pass-through to the next module. The secondary channel is an additional point-to-point serial link. This results in a total of 48 high-speed serial channels.
- The primary channels are routed on the top side of the memory module using microstrip. Trace lengths vary from approximately 2-7in. The secondary channels are routed on the backside of the module and transition first into a stripline layer and then to the top of the module where they interface with the AMB BGA.
- For our investigation we will focus on the first channel of the Primary South and Secondary South channels. We will show the end-to-end channels for two configurations: host memory bridge to AMB and AMB to AMB.
- Passive channels will be extracted for the packages, the motherboard, the FB-DIMM connector, and module routing.
- Transistor level active drivers were developed with de-emphasis to meet the FB-DIMM spec.
- The following slide shows a block diagram of the system to be extracted, simulated, and validated along with the applicable Ansoft simulation tools.

Model Extraction



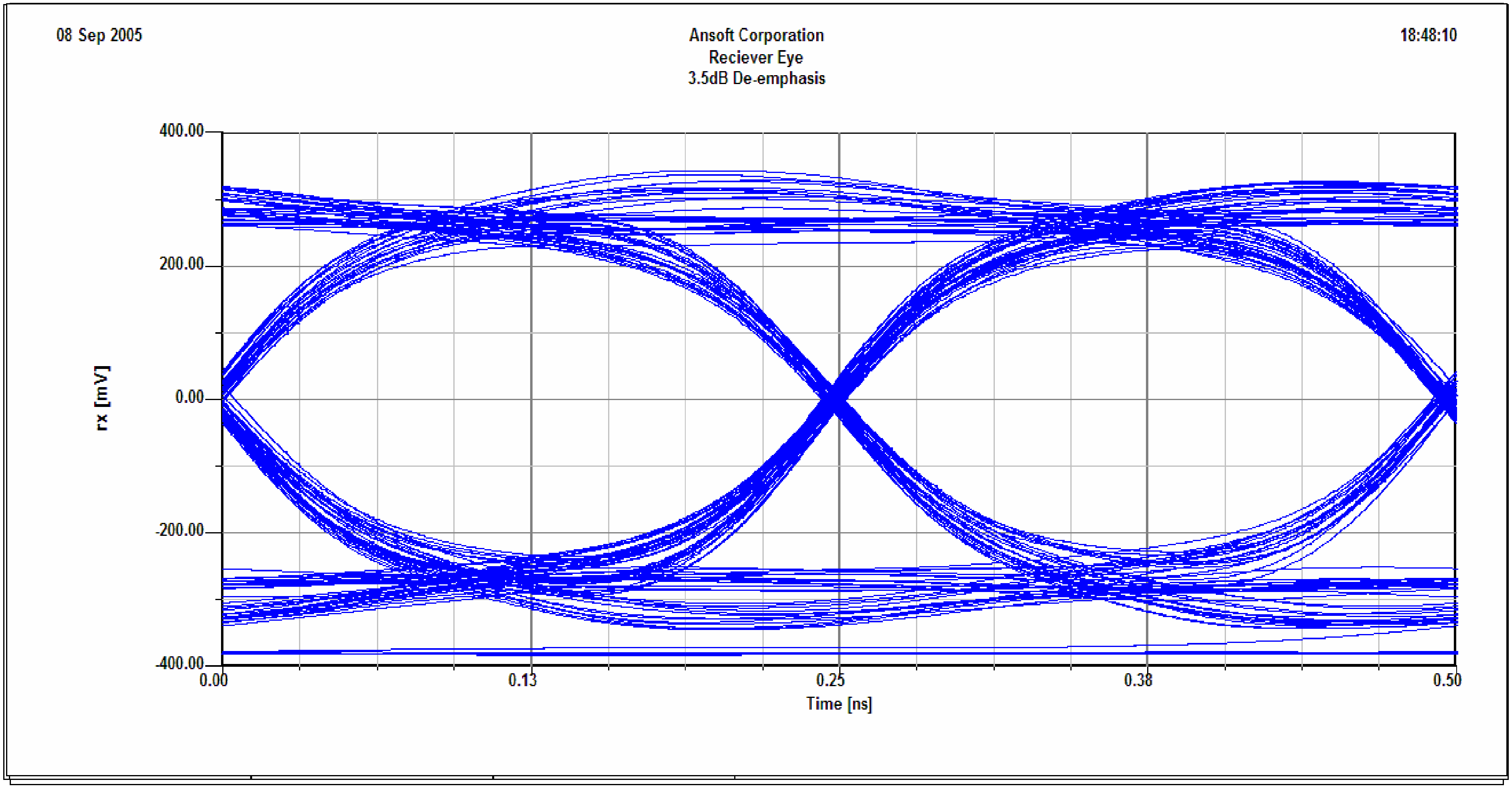
De-emphasis at work!

- FB-DIMM board (Primary South Side)



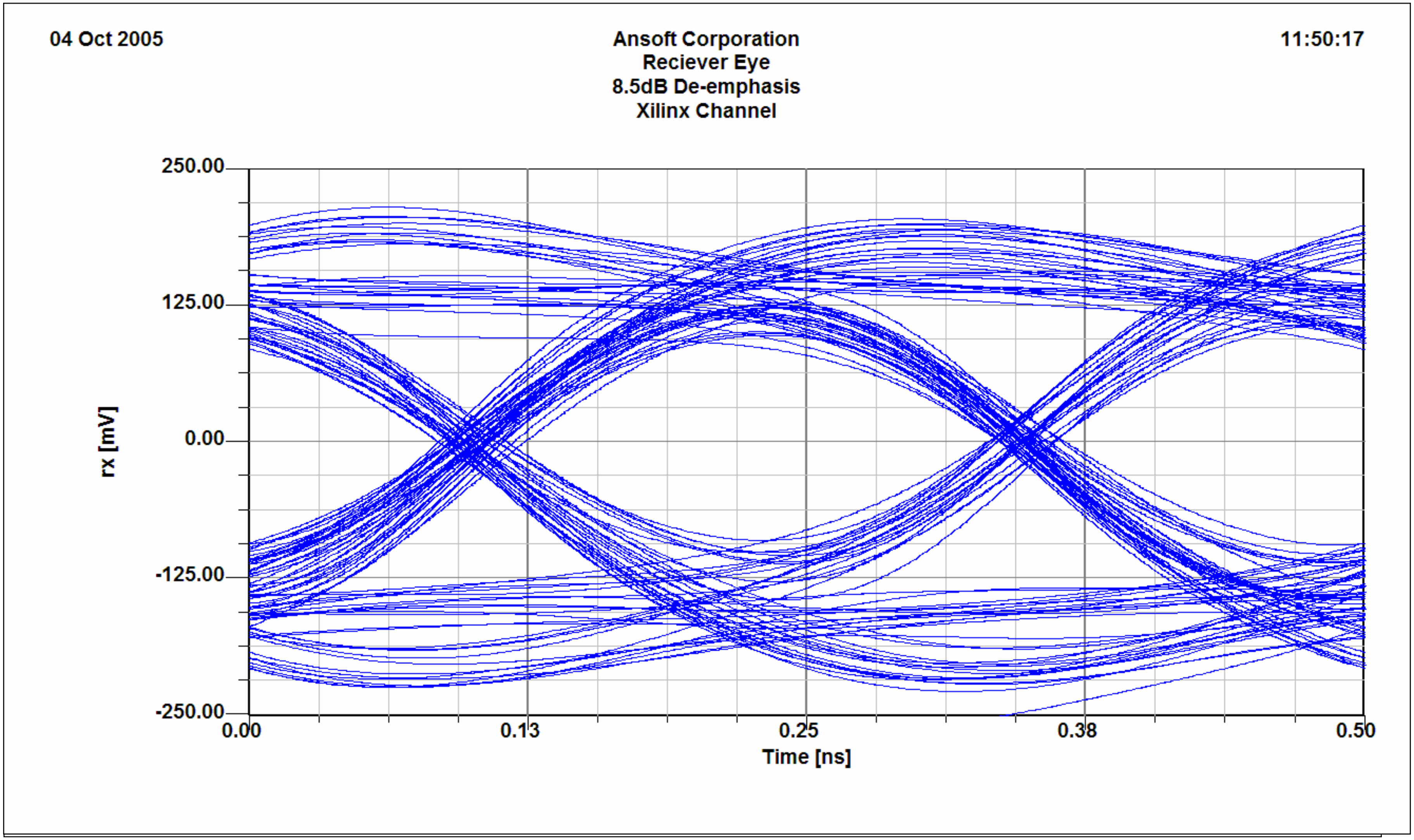
De-emphasis at work!

- Xilinx Virtex II Pro test board



De-emphasis at work!

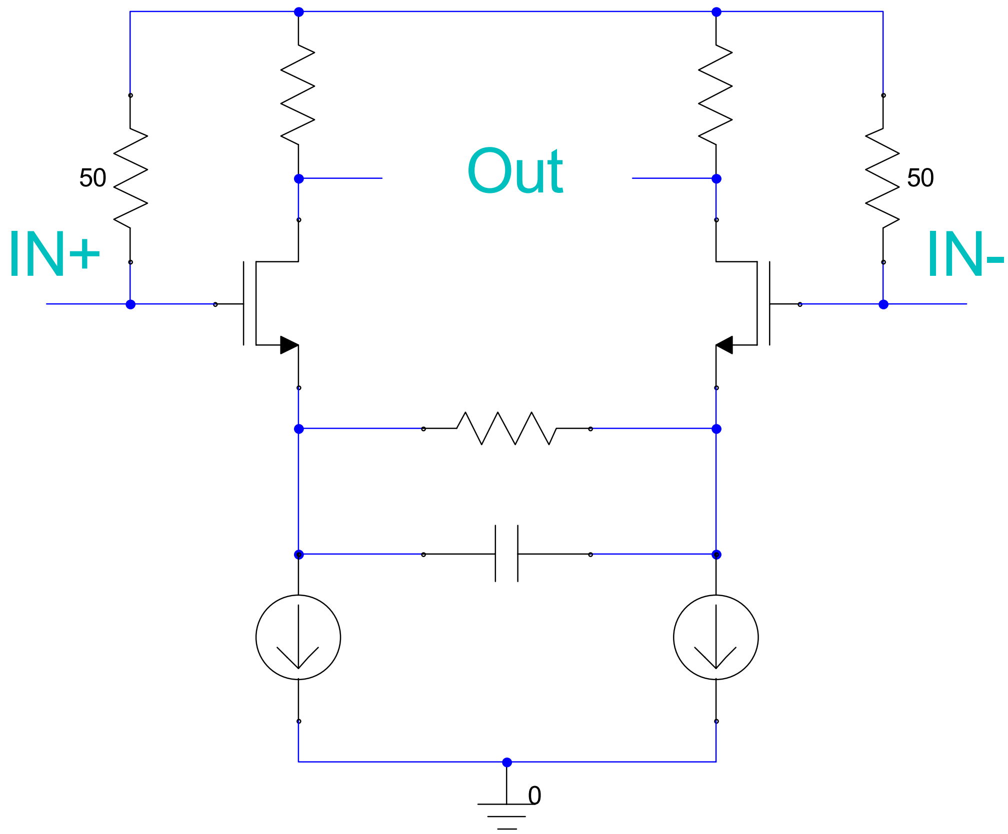
- Two Xilinx Virtex II Pro test boards in series
- Increased De-emphasis to improve performance



Receive Equalization

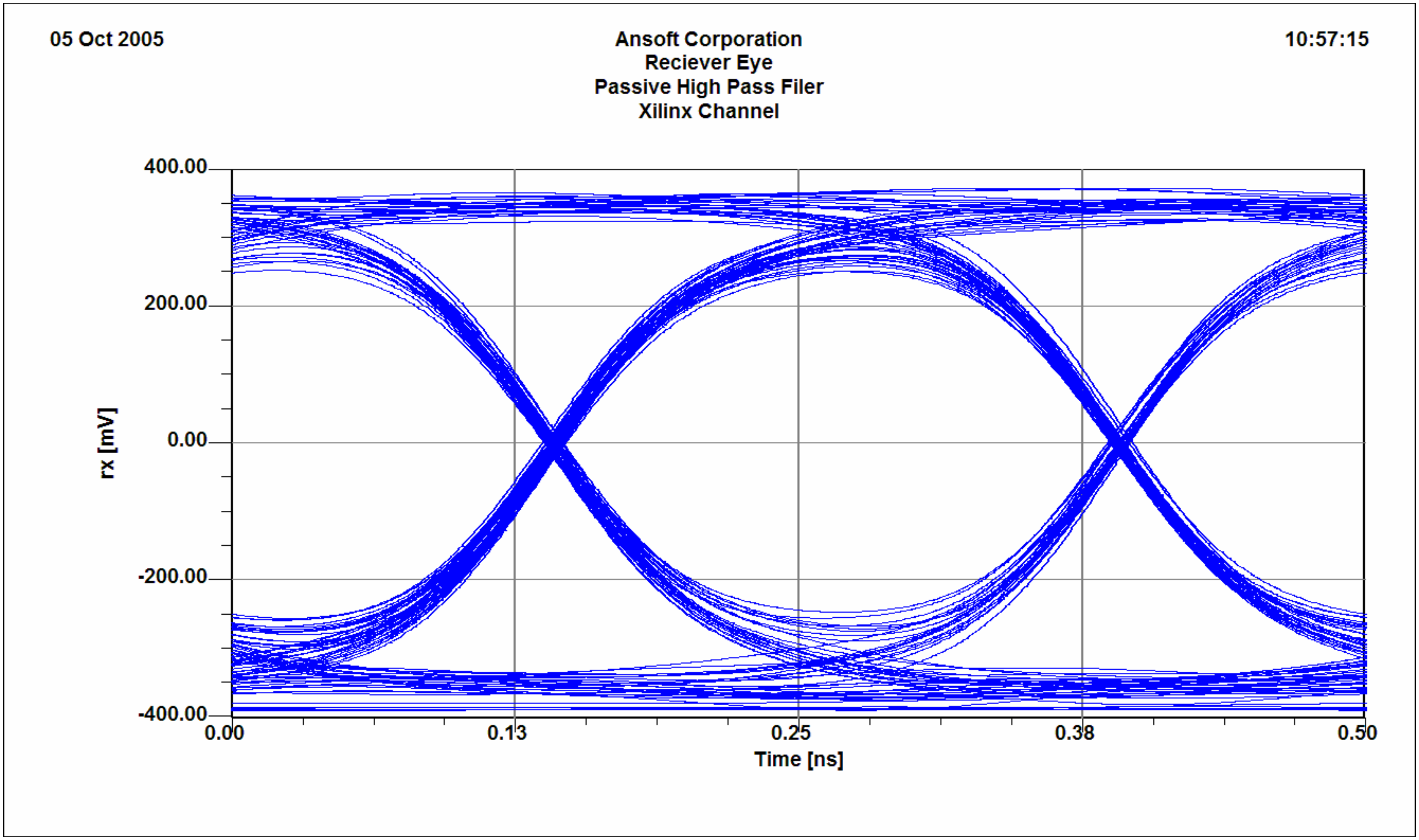
- Passive Network
- Adaptive Equalization can incorporated

Incorporating passive network into reciever to maintain 50 Ohm matching



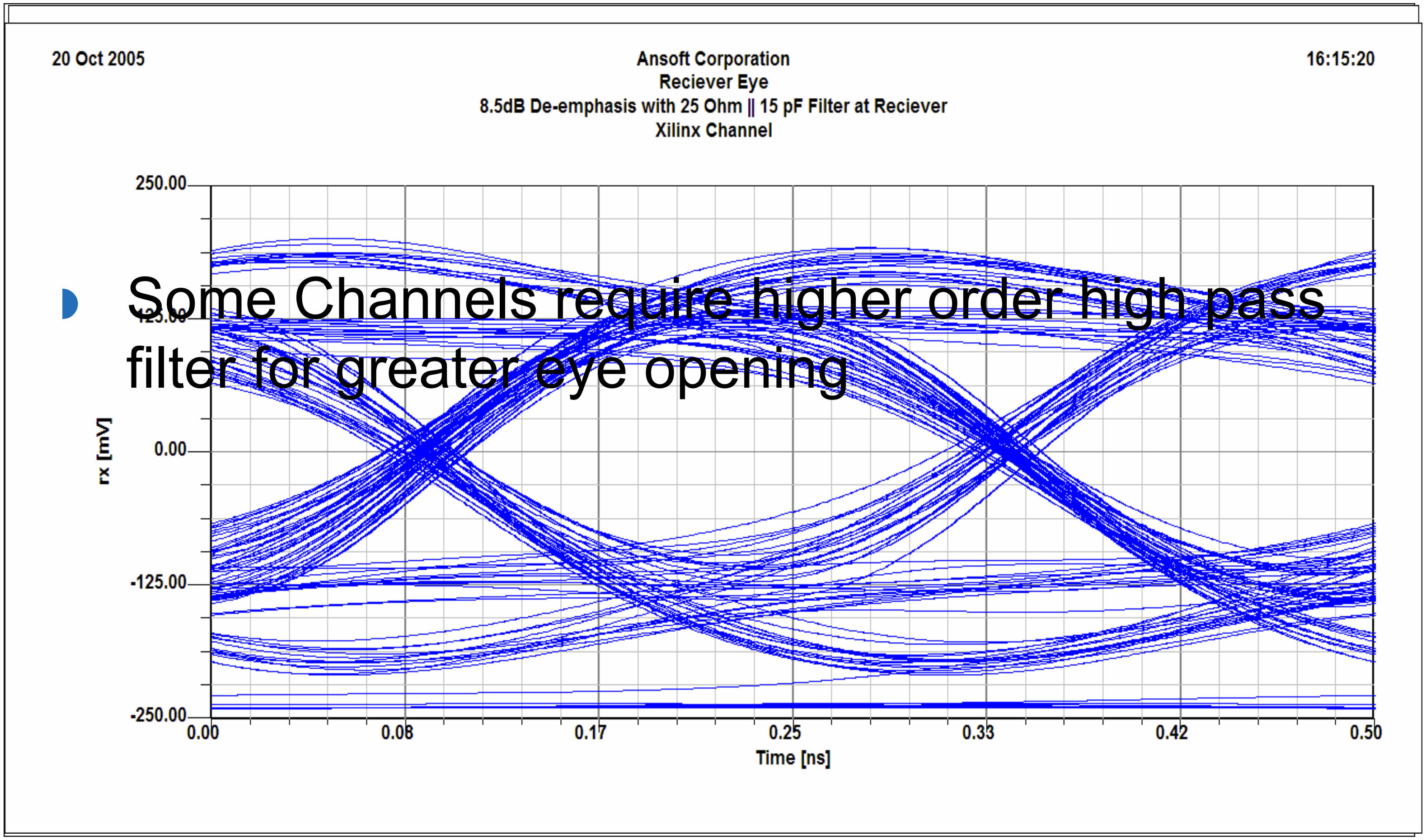
Receive Passive Equalization

- Xilinx Virtex II Pro test board



Combination of De-emphasis and Receive Equalization

- Two Xilinx Virtex II Pro test boards in series



- Some Channels require higher order high pass filter for greater eye opening

Summary

- Outlined challenges faced in high speed serial interconnects
- Discussed Equalization techniques
- Presented a De-emphasis circuit that is compliant with FB-DIMM standard
- Simulations (Nexxim) show the benefits of using De-emphasis
- Example of a simple Receive equalization technique
- Example of a combination of De-emphasis and Receive equalization
- Demonstrated diminishing returns from simple low order equalization circuits for a channel with higher order properties
- Ansoft has come out with a well integrated design kit that includes
  - Channel Modeling: Trace/Backplane, Vias, Connectors
  - Transceiver design with equalization techniques to enhance high speed data transmission over Copper
- Work with board designers to solve their signal integrity issues to ensure high signal quality for data recovery