Design and Optimization of a Broadband Surface Mount Package

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Agenda

- Ceramic technologies for broadband surface mount packages
- Technology Selection
- Design of a broadband surface mount package
- Conclusions

Ceramic Technologies for Broadband Surface Mount Packages

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Available Ceramic Technologies

Well Established

- **Thin-Film**
  - Sputter and etch process
  - Small size, light weight, good thermal
  - Broadband performance
  - Integrated passives
- **HTCC**
  - Similar to Thick-Film, uses lossy metal (W, Mo/Mn) as conductors
  - Multilayer capability
  - Limited to microwave frequencies
- **Thick-Film**
  - Uses various inks pressed through patterned silk screen
  - Cost effective, limited to microwave frequencies
  - Integrated passives
- **Bonded Plated Copper**
  - Semi-additive copper plating process, combined with photolithography
  - Fine lines (3mil) and dense copper circuitry on ceramic

Relatively New

- **LTCC**
  - Uses glass ceramics and high conductivity metals for low loss, high-performance
  - Integrated passives offer high flexibility
  - Multilayer capability
  - Photoimageable dielectrics and metals
- **Etched Thick-Film**
  - Performance comparable to thin-film
  - Uses thick-film materials
  - Integrated passives
  - Capable of a small number of layers

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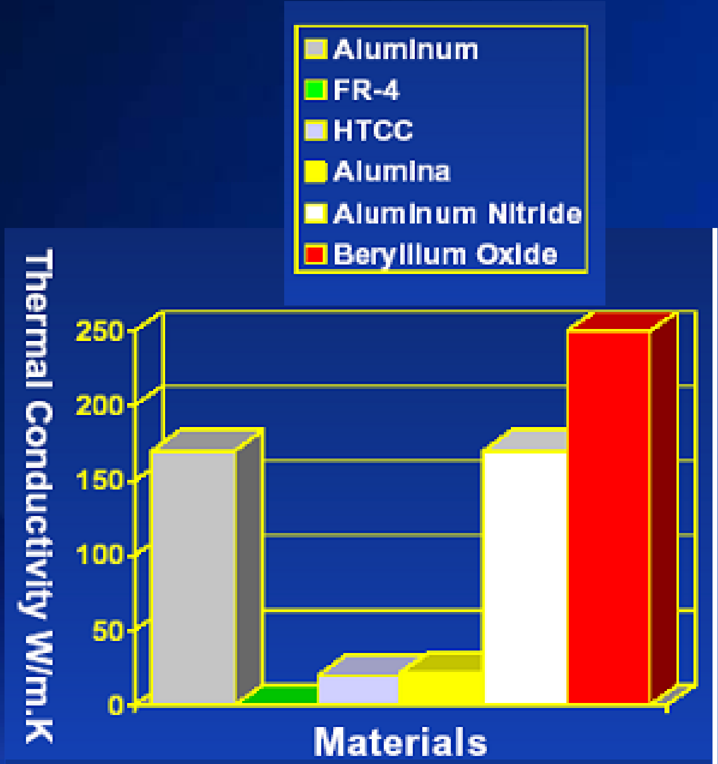
Why Ceramic?

- **Advantages**
  - Stable properties (ε_r, $\tan(\delta)$) vs. temperature
  - Wide range of dielectric constant value and losses, metal systems
  - Precision fabrication capability (line width and spacing)
  - Low loss at microwave frequencies
  - Integrated Passives (RLC)
  - Low, stable CTE, matched to GaAs, InP and Silicon
  - HiCTE glass ceramic is also offered to match PWB CTE
  - Superior thermal performance
  - High reliability, proven field life
  - Hermeticity
- **Limitations**
  - Substrate Size
  - Lead time (Thick-Film, HTCC, LTCC)
  - NRE Cost (HTCC, LTCC)



- High thermal conductivity:–
  - Alumina 100 times FR4
  - LTCC 20 times FR4
  - Thermal vias can be included
  - LTCC allows heat pipe approach

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Typical Materials Properties

- Substrates and heat spreaders for Thin-Film, Thick Film, HTCC, and Etched-Thick Film

Material	Composition	Density (g/cm^3)	CTE x 10^{-6}/K (25° to 150°C)	Thermal Conductivity (W/m-K)	Available Forms
Al-SiC	Al + 50 to 67% SiC	3.00	6.5 to 9.0	160	Net-shape
CuW	W + 11 to 20% Cu	15.65 to 17.00	6.5 to 8.3	180 to 200	Sheet/Billet
CuMo	Mo + 15 to 20% Cu	10.00	7.0 to 8.0	160 to 170	Sheet/Billet
Al-Si	60Al-40Si	2.53	15.4	126	Sheet/Billet
Kovar	Fe-Ni	8.10	5.2	11 to 17	Sheet/Billet
Cu		8.96	17.8	398	Sheet/Billet Rod
Al		2.70	23.6	238	Sheet/Billet Rod
Si		2.30	4.2	151	IC Chip
GaAs		5.32	6.5	54	IC Chip
Al_2O_3		3.60	6.7	17	Substrates
BeO		2.90	7.6	250	Substrates
AlN	98% Purity	3.30	4.5	160 to 200	Net-Shape
InP		4.79	4.6	80	IC Chip

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Technology Selection

Requirements for High-Speed Signals

- Dielectric losses increase rise and fall time of a switching signal
  - Propagation of fast edges requires use of material with low dielectric loss at high frequency
  - 10 ps rise/fall (20%-80%) => signal BW~22GHz
  - 10 ps rise/fall (10%-90%) => signal BW~35GHz
  - 10 ps rise/fall (10%-90%) => signal BW~23.5GHz
- Attenuation due to dielectric losses is proportional to $\varepsilon_r \times \tan(\delta)$
  - Materials with low ε_r
- Metal losses prolong the tail of the signal edges
  - Low loss conductors (Au, Ag)
- Multilayer capability is desirable for shielding of high-speed traces, and is necessary for ICs with high I/O count
- Three technologies have the above requirements
  - Etched Thick Film
  - LTCC
  - HTCC

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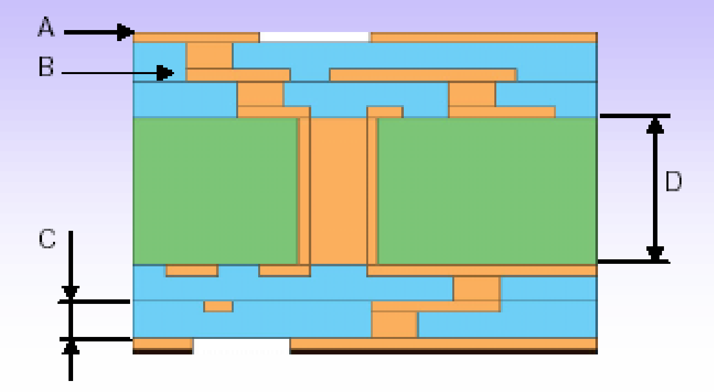
Etched-Thick Film

- Features
  - thin-film scale geometries 25um w/s
  - Dense fine lines with Ag & Au conductors
  - Solid filled vias
  - Multilayer, precision layer to layer alignment
- Applications of ECP technology include
  - Optoelectronics: Tx, Rx, Modulators, Switches, Mux, Demux, Drivers
  - Military & Aerospace: Radar modules, guidance modules, communication modules
  - Wireless Communications: Point-to-point radios, point-to-multi point radios, satellite communication module



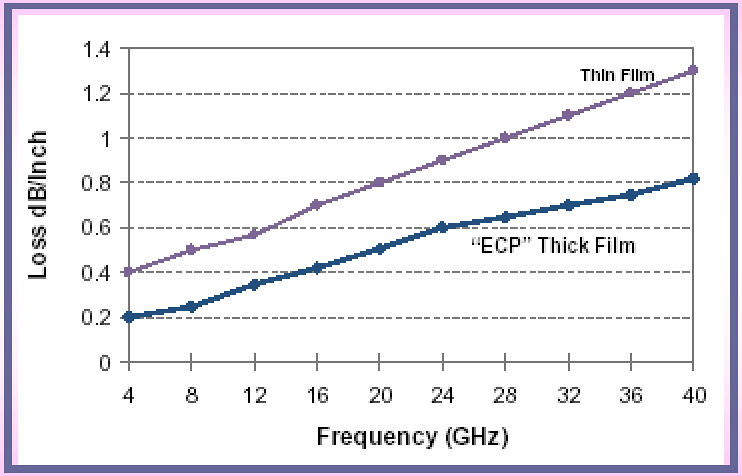
ITEM	DESIGNATION		STANDARD DESIGN RULES	
			Thick Film	ECP
A,B	Au Surface/ Internal Conductor Thickness	1	10µm ±2µm	4~6µm
		2		6~8µm
	Ag Surface/ Internal Conductor Thickness		10µm ±2µm	9~12µm
A	. Au-Pt-Pd Surface Conductor Thickness . Ag-Pd Surface Conductor Thickness		18µm 15µm	NA NA
C	Dielectric Thickness		40µm ± 10µm	40µm ± 5µm
D	Ceramic Core Thickness		0.254~1.016mm [.010"~.040"]	

ECP Compared to Thin Film

	ECP Technology	Standard Thin-Film
Frequency	Through 94GHz	Through 94GHz
Line Width	25um	25um
Multi-layer capability	Higher layer count	Limited layer count
Air Bridges	High repeatability	Low repeatability
Electrical modeling	Single material conductive layer	Multiple material conductive layers
Resistors	Yes (<=100M?Sq.)	Yes (limited range)
Capacitors	Yes (wide range)	Yes (limited range)

- ⇨ 30-50% Lower S_{21} Loss
- ⇨ Thru 94 GHz
- ⇨ Low Line Resistivity

Insertion Loss Improvement



Advantages of "ECP"

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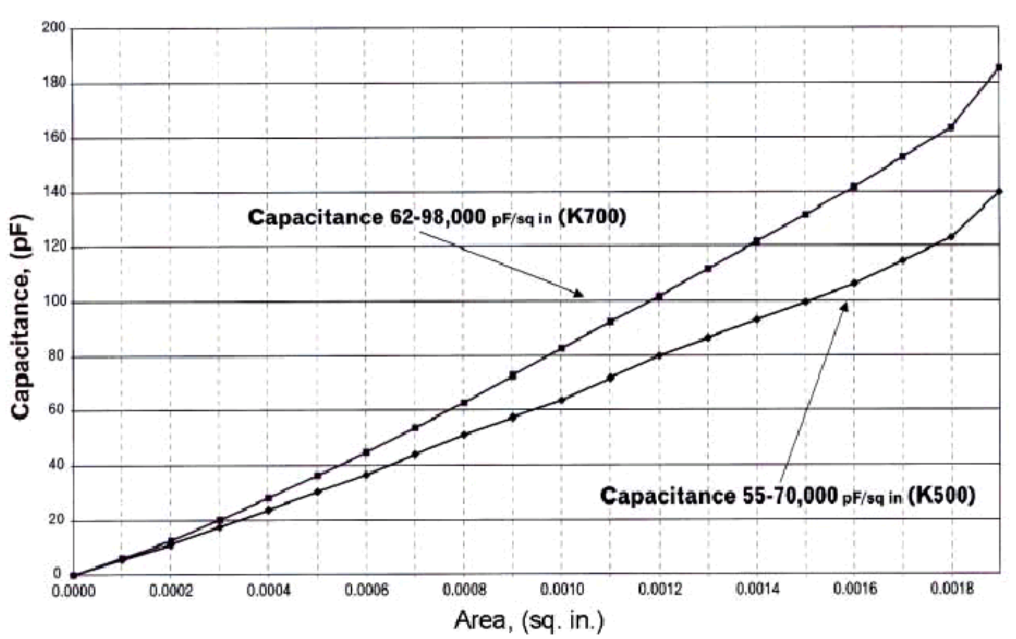
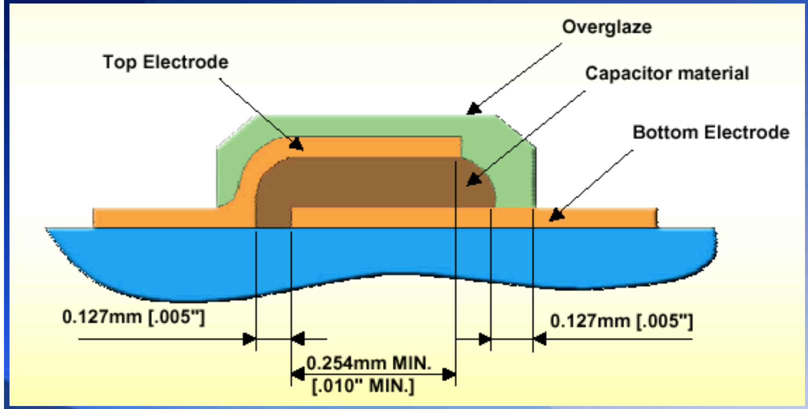
ECP Compared to LTCC

	ECP Technology	LTCC
Frequency	Through 94GHz	Through 94GHz
Line Width	25um	100um
Line Spacing	25um	100um
Via Diameter	75um	150um
Layer Alignement	12.5um	25um
Resistors	Yes, some photoimageable	Yes
Capacitors	Yes (wide range)	Yes (wide range)





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Typical LTCC Materials Properties

Property	DuPont 951	DuPont 943	Ferro A6-M	Ferro A6-S	Heratape CT 700	Lamina Cu/Mo/Cu	Lamina CuW
Available Fired Thickness (mils)	3.7, 5.2, 8.2	4.5	3.7, 7.4	3.7, 7.4	3.6, 5.7, 7.9	5	4.5
Dielectric Constant (K)	7.8 @ 10MHz	7.5	5.9	5.9	7.9	5.5 @ 15GHz	6.4 @ 16GHz
Dielectric Loss	0.0015 @ 10MHz	0.001 @ 40GHz	0.002 up to 50GHz	0.002 up to 50GHz	0.002 @ 1KHz	0.0006 @15GHz 25°C	0.024 @16GHz 25°C
T.C.E. (ppm/°C)	5.9	6	7	8	6.7	5.5	6
XY Shrinkage	13± 0.2%	9.5 ± 0.3%	14.8 ± 0.2%	14.9 ± 0.2%	14.4 ± 0.3%	0 ± 0.1%	<0.5%
Z Shrinkage	15±0.5%	10.3±0.5%	25±0.5%	24±0.2%	14.9±0.8%		
Metallization	Au/Ag - Ag - Au	Au/Ag - Ag - Au	Au/Ag - Ag - Au	Au/Ag - Ag - Au	Au/Ag - Ag - Au	Ag - Au	Ag - Au
Flexural Strength (Kpsi)	28.3 (320 Mpa)	33.4	17.1	(14.15) 160 Mpa	(21.22) 240 Mpa		
Thermal Conductivity (W/mK)	3	4.9	2	2	4.3		

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Low Resistance Conductors Alumina

Material Characteristics

			LTCC				Low Resistance Alumina	Alumina
Ceramic Material			GL530	GL550	GL560	GL660	AO600	A473
			Prototype Production	on Volume Production	on Volume Production	on Volume Production	on Volume Production	
(Feature)			Low ε LowTanδ	Low ε	Low ε	High ε	Low R, High Strength, High Thermal-Conductivity	
			PB FREE	Pb FREE	Pb FREE	Pb FREE	Pb FREE	
Conductive Material			Cu	Cu	Cu	Cu	$Cu_{+\alpha}$	W
Material Characteristics	ε(3.2GHz)		4.9	5.6	6	9.5	8.7	8.8
	ε(60GHz)		4.9	5.7	(6)	-	8.8	8.6
	Tanδ(3.2GHz)	$\times 10^{-4}$	8	12	17	16	17	12
	Tanδ(60GHz)	$\times 10^{-4}$	11	19	(35)	-	13	21
	C.T.E.	40-400degreeC	5.5	5.9	7.9	6.2	7.2	7.8
	Thermal Conductivity	W/mK	1.4	2.0	1.2	1.3	15	19
	Bending Strength	Mpa	200	250	200	200	400	400
	Sheet Resistance	mohm/SQ.	3	3	3	3	4(2)	8

Courtesy: Kyocera Corporation

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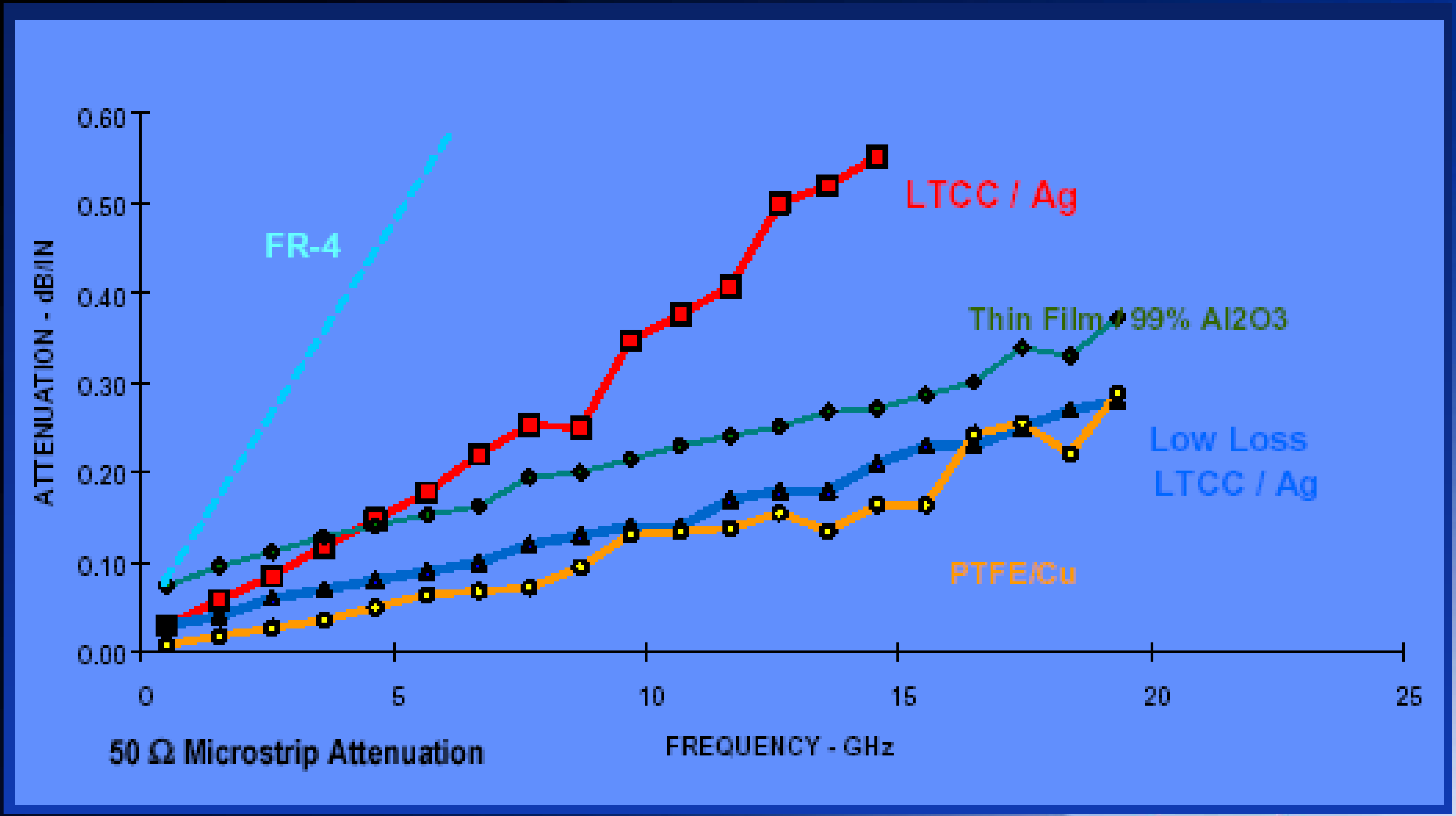
Line Loss Comparison
Ceramic vs. Competing Material



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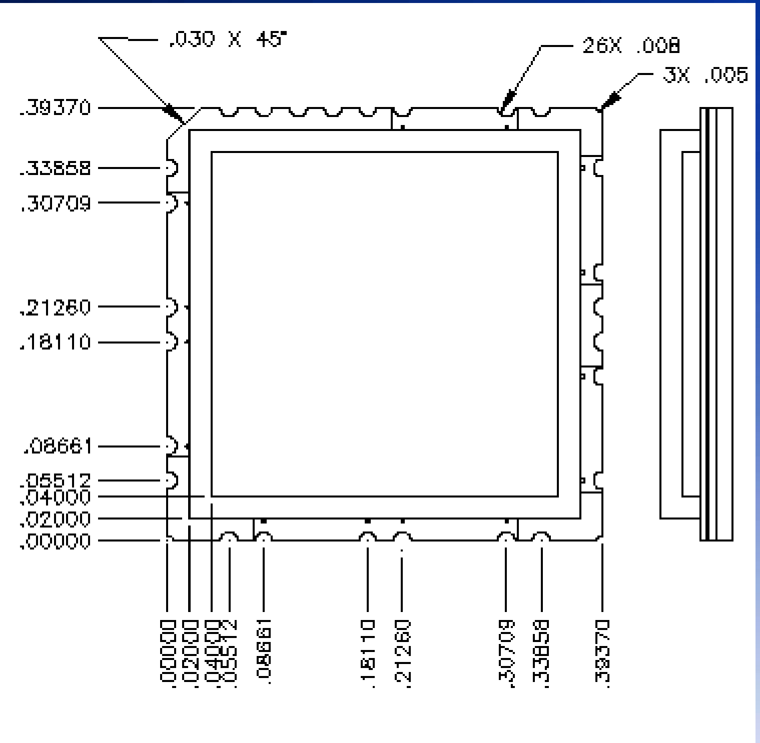
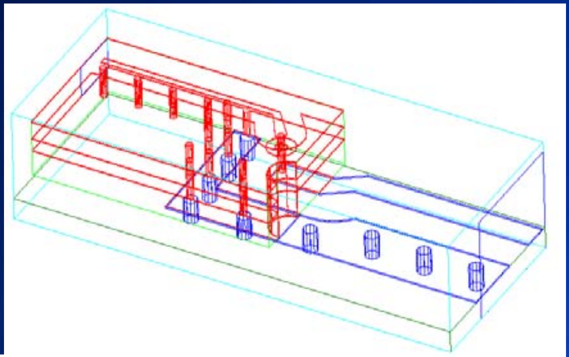
Effect of Manufacturing Tolerances

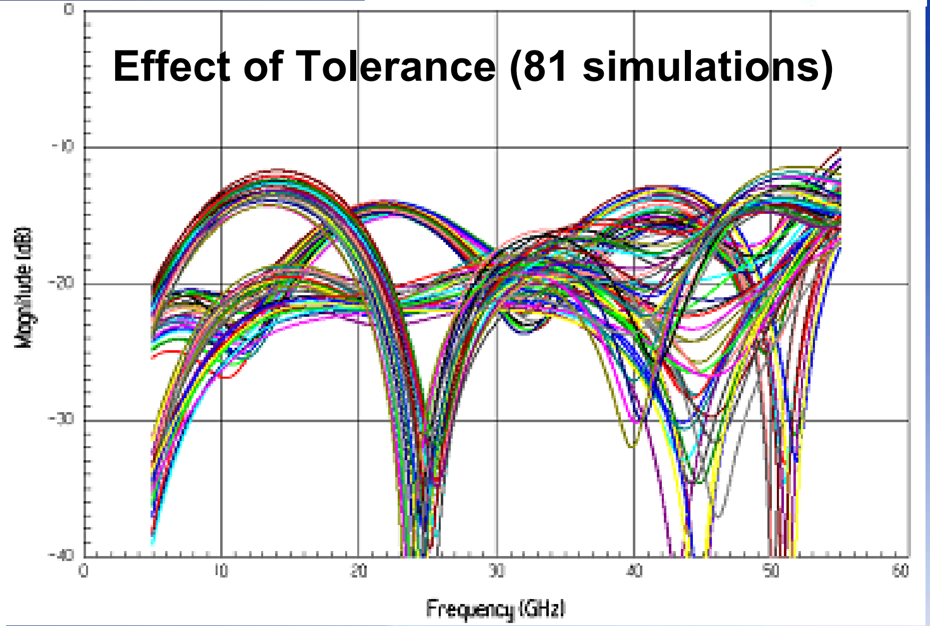
- Case study: 10mm sq. LCC package for applications at 40Gb/s
  - High-speed signal vias and lands are designed to minimize return loss for differential signaling
  - Return loss and insertion loss are affected by:
    - Thickness of three ceramic layers
    - Line width
  - Nominal Design in three different technologies
  - Effect of tolerance intrinsic to each technology/vendor

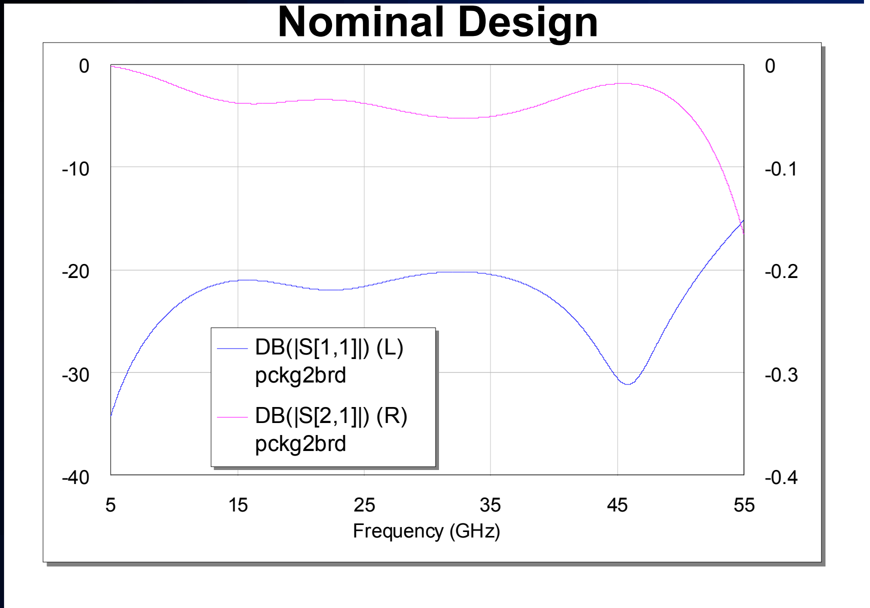


Effect of Manufacturing Tolerances

- HTCC
  - Nominal design has Input return loss < -20dB up to 50GHz
  - Ceramic tape thickness tolerance ±10%
  - Line width tolerance ±1mil







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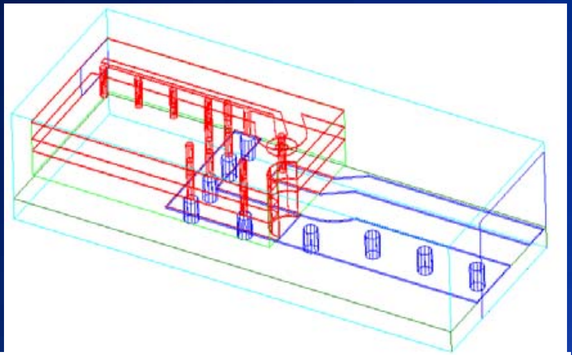
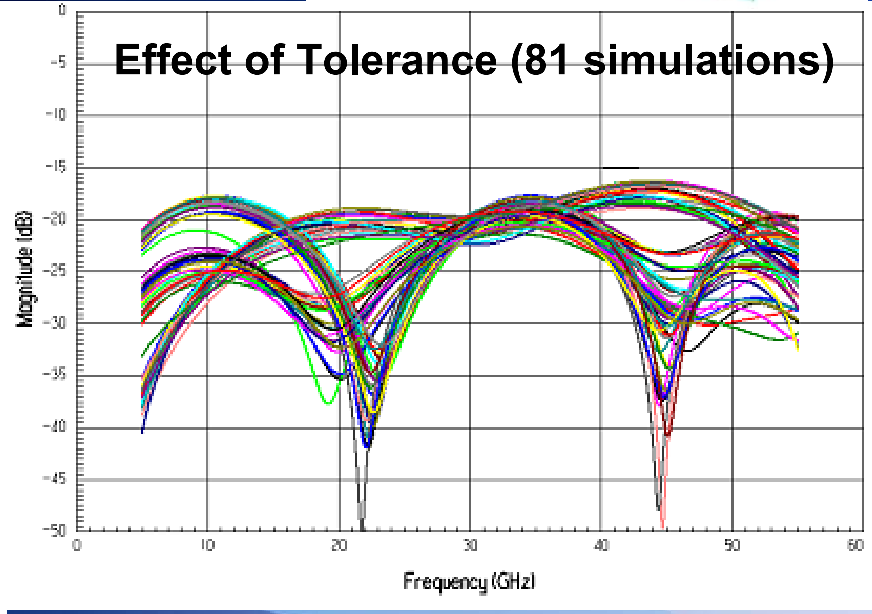
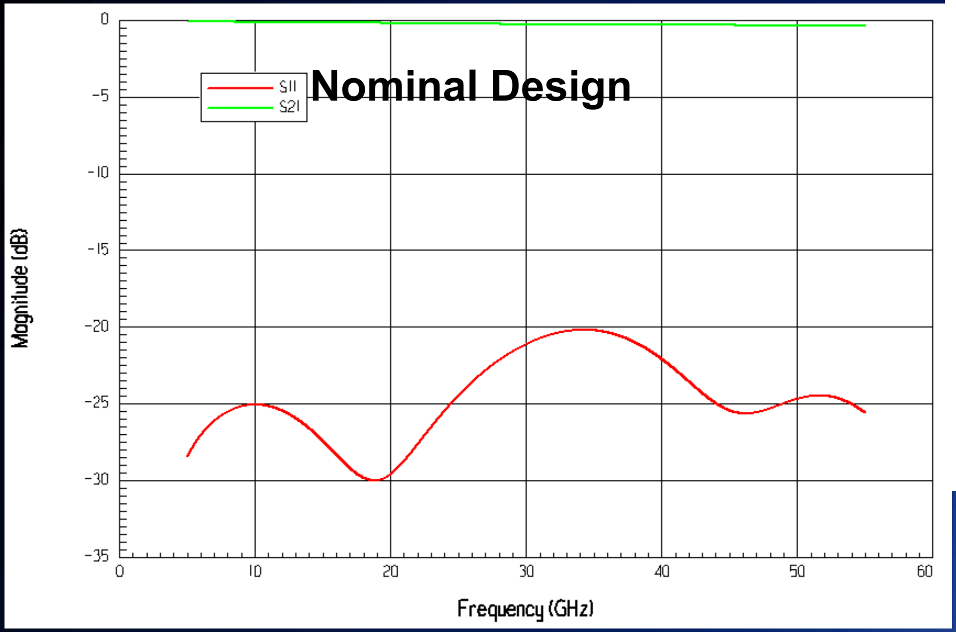
Effect of Manufacturing Tolerances

- LTCC
  - Nominal design has Input return loss < -20dB up to 55GHz
  - Ceramic tape thickness tolerance ±10%
  - Line width tolerance ±0.5mil







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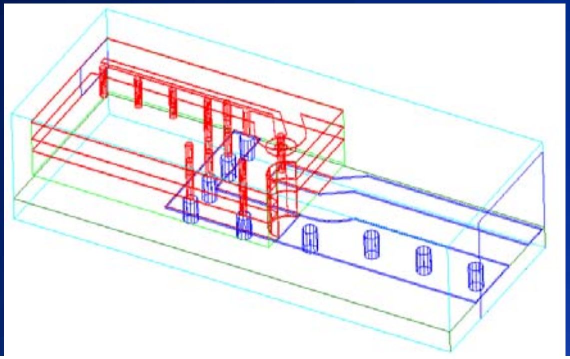
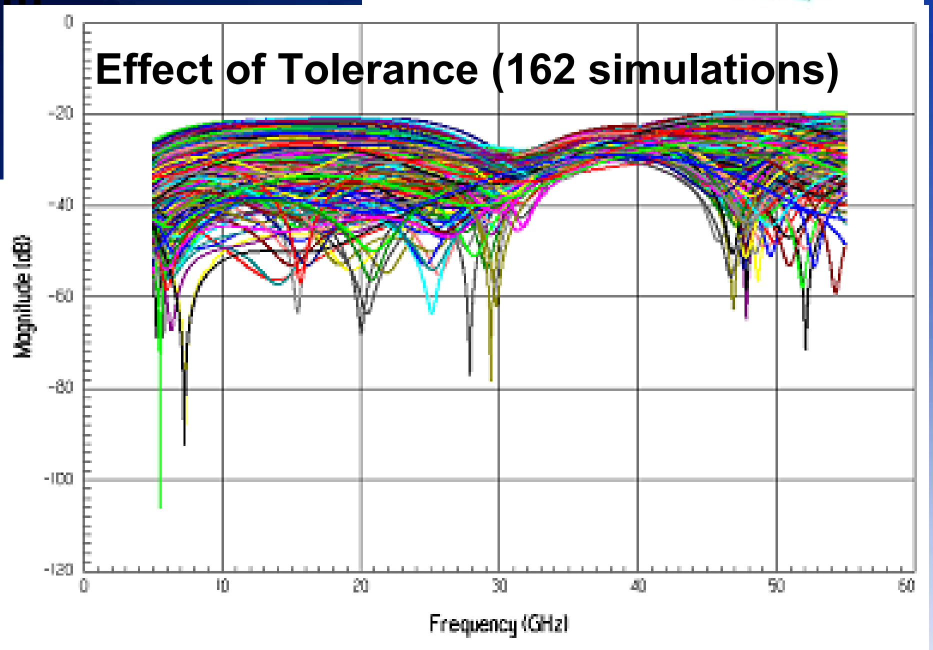
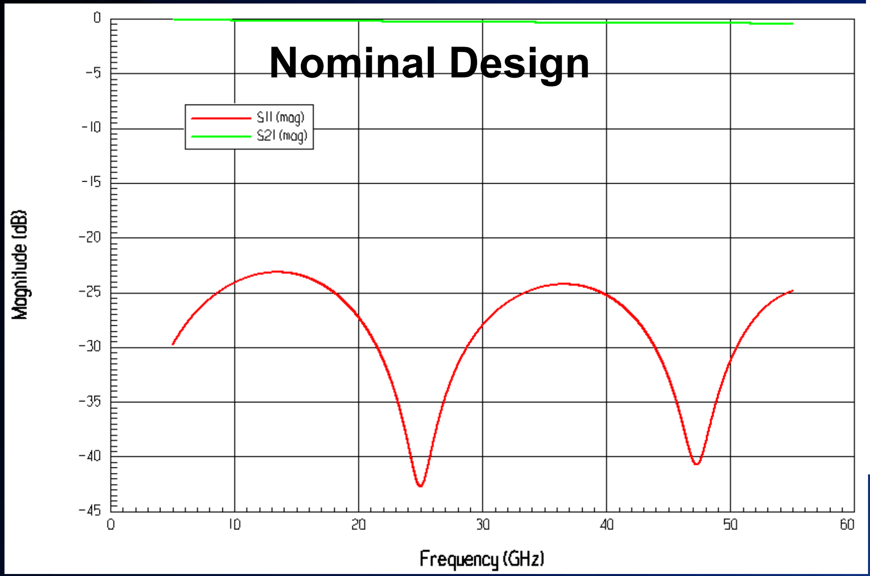
Effect of Manufacturing Tolerances

- Etched Thick-Film
  - Nominal design has Input return loss < -20dB up to 55GHz
  - Ceramic tape thickness tolerance ±10%
  - Line width tolerance ±0.2mil
  - Trace thickness tolerance ±2μm







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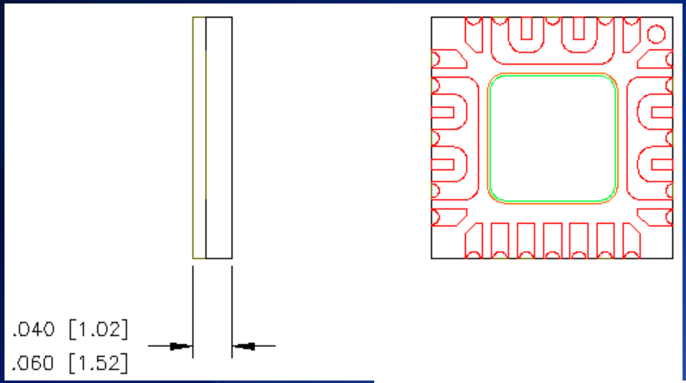
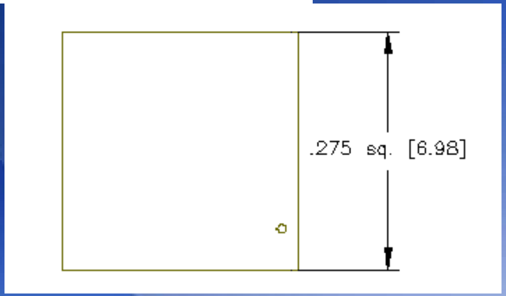
Design of a broadband surface mount package

LGA Package for 25Gb/s High-Speed Logic ICs

- Die Characteristics
  - InP HBT technology
  - Dimension: 1.280mm X 0.980 mm
  - Thickness: 6 mil
  - Max power : 0.5W @ º85C
- Package Requirements:
  - Mechanical:
    - Surface Mount
    - Hermetic Package
  - Thermal
    - Max operating package case temperature: 85ºC
    - Max operating junction temperature: 150ºC
  - Electrical
    - On-package decoupling caps
    - S11 < -12dB up to 25GHz (packaged die)
    - S22 < -10dB up to 25GHz (packaged die)
    - S21 > -1dB up to 25GHz (package only)





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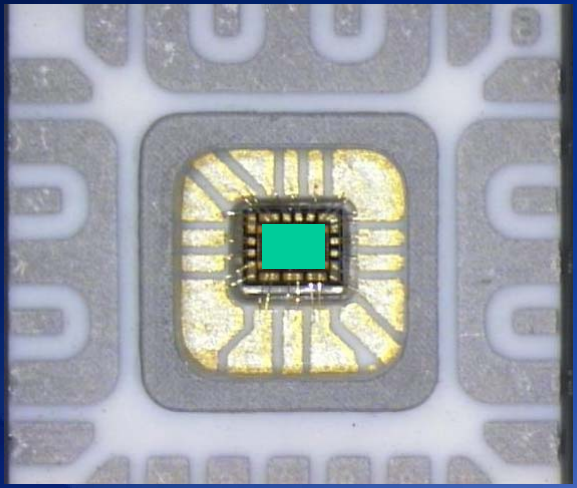
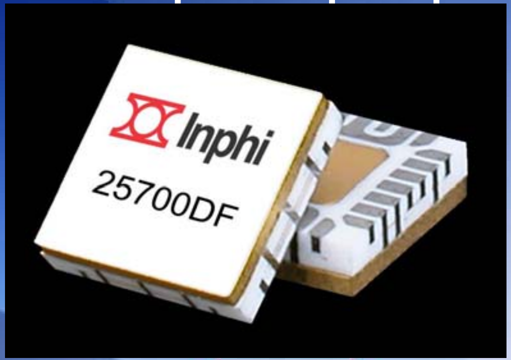
Package Structure

- Package architecture & technology
  - CD LGA with wire bonds
  - 7x7 mm LTCC hermetic package
- Electrical Design
  - Die is recessed in a cavity to minimize bond wire length
  - Decoupling caps buried in LTCC
  - All transitions optimized using full-wave EM simulations
    - Wire-bonds
    - Coupled microstrip to stripline
    - Package-to-board transition



25 Gbps D Flip-Flop



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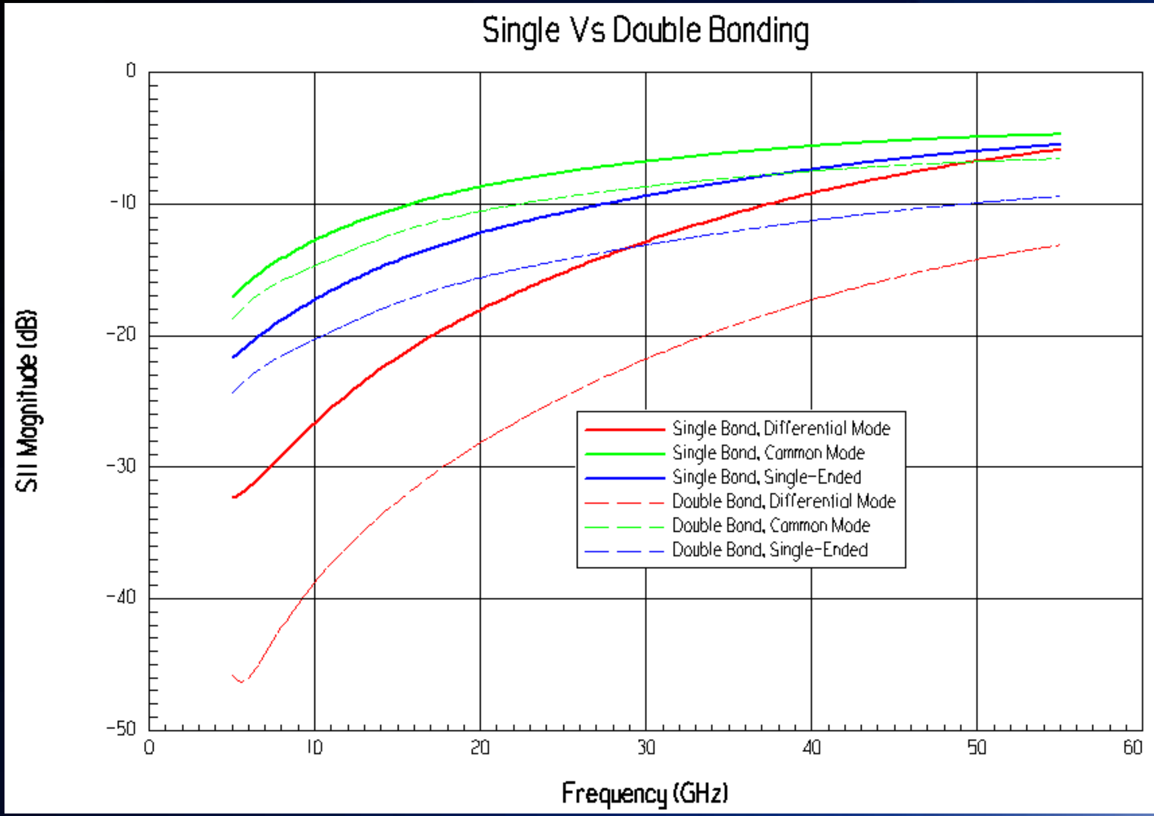
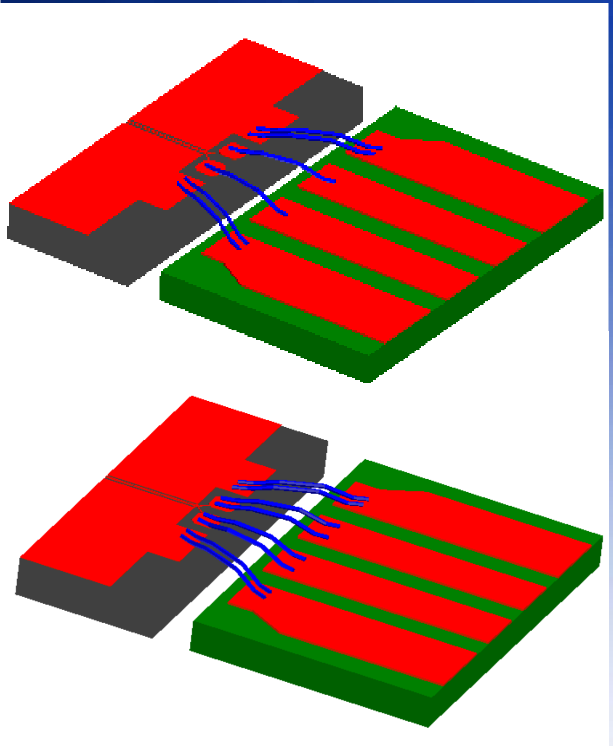
Single vs. Double Bonding

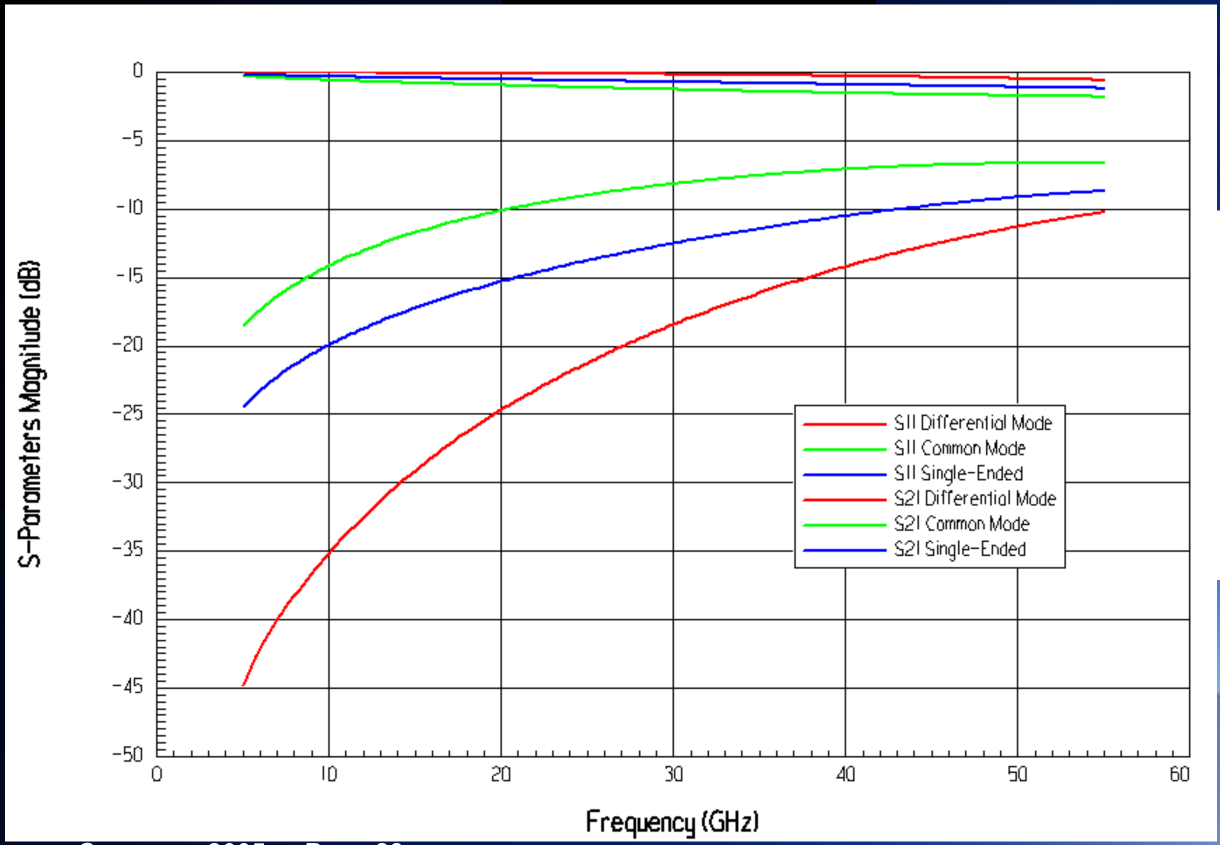
- Chip thickness: 6mil
- Package shelf thickness: 5 mil
- Gap width: 6mil
- Bond Wires diameter: 0.7 mil
- Edge bonding with 1 mil loop height
- No backside metal on-chip
- GCPW on package shelf
- Ceramic dielectric constant: 5.5

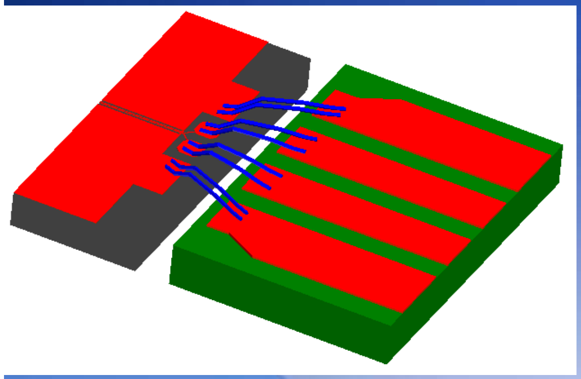




Wire Bonds and Different Signaling Conditions

- Chip thickness: 6mil
- Package shelf thickness: 7.4 mil
- Gap width: 6mil
- Bond Wires diameter: 0.7 mil
- Edge bonding with 1 mil loop height
- No backside metal on-chip
- GCPW on package shelf
- Ceramic dielectric constant: 5.9





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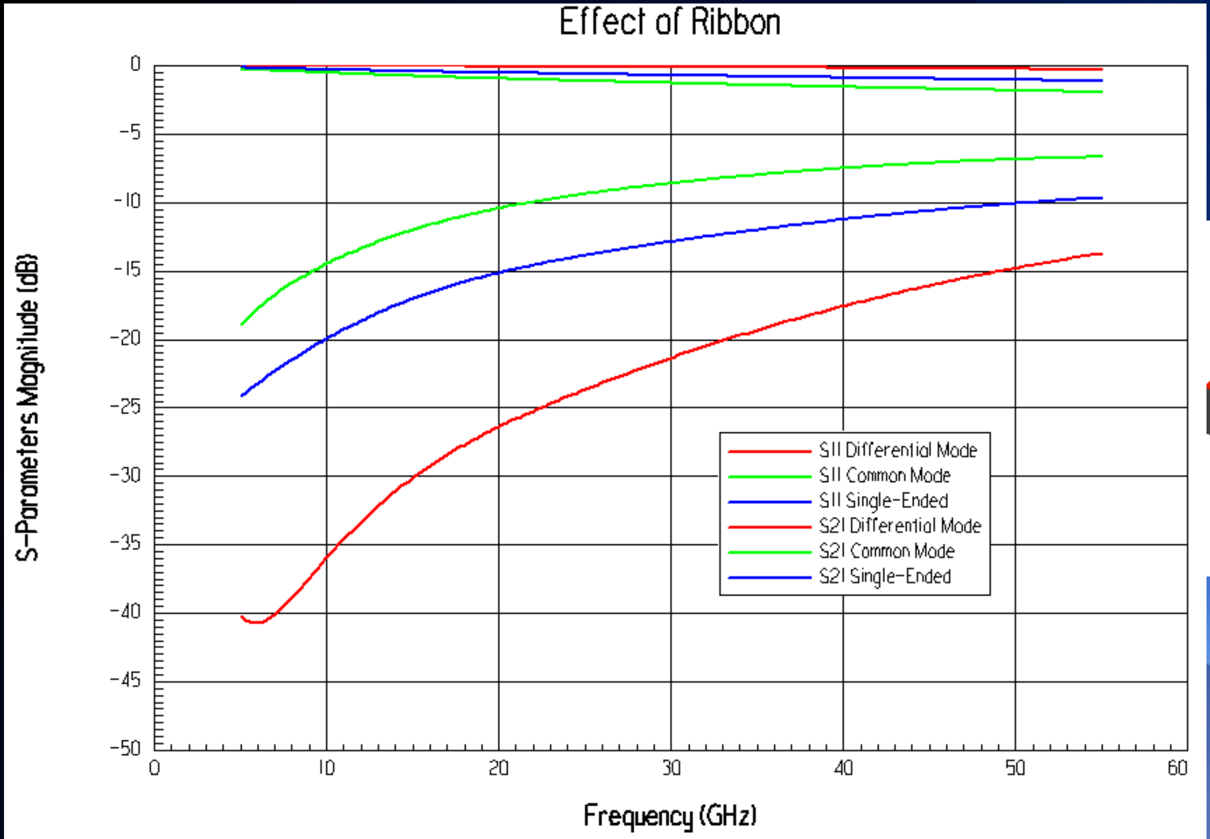
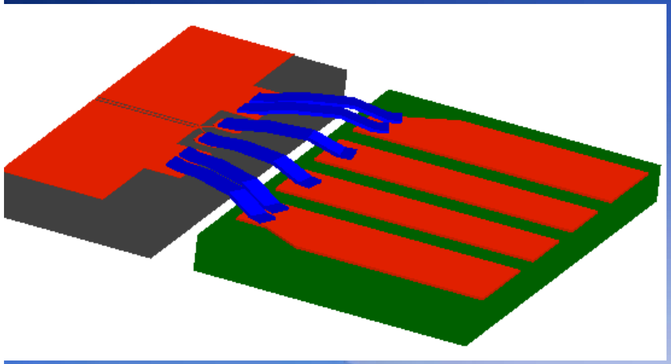
Ribbons and Different Signaling Conditions

- Chip thickness: 6mil
- Package shelf thickness: 5 mil
- Gap width: 6mil
- Ribbons dimension: 0.5 mil X 3 mil
- Edge bonding with 1.5 mil loop height
- No backside metal on-chip
- GCPW on package shelf
- Ceramic dielectric constant: 5.5





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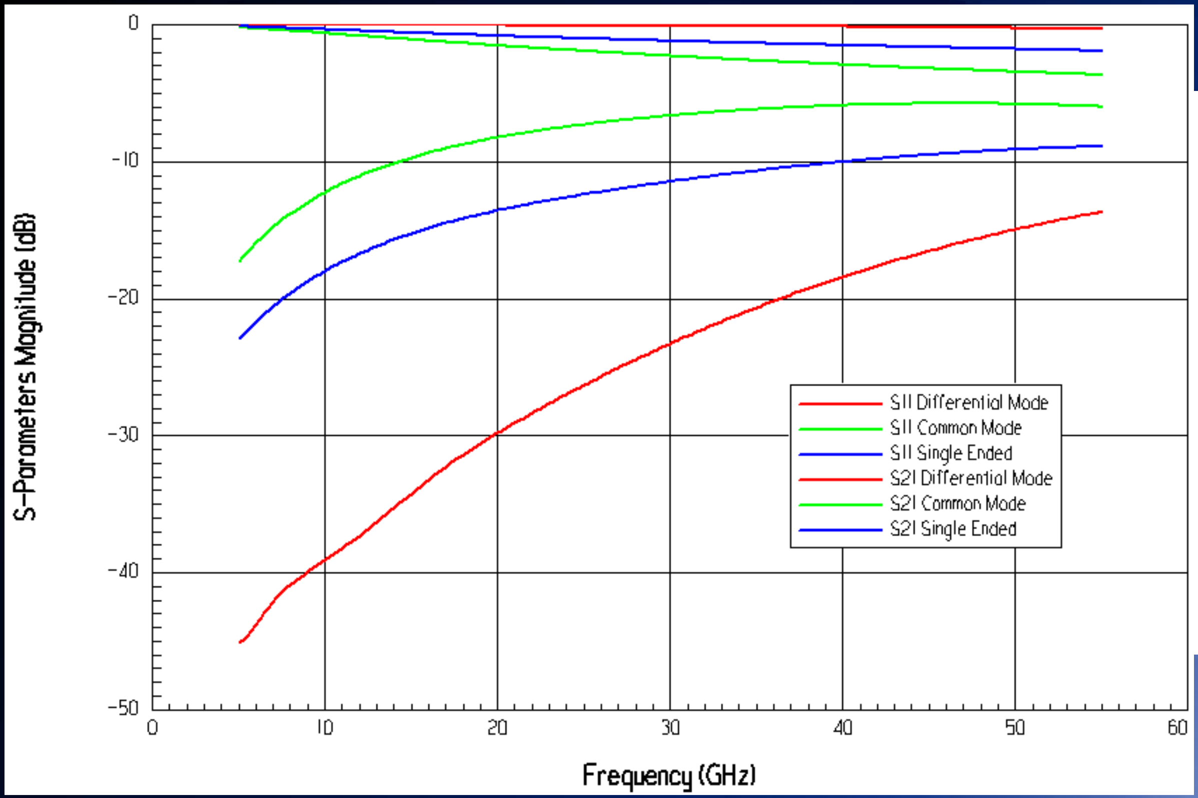
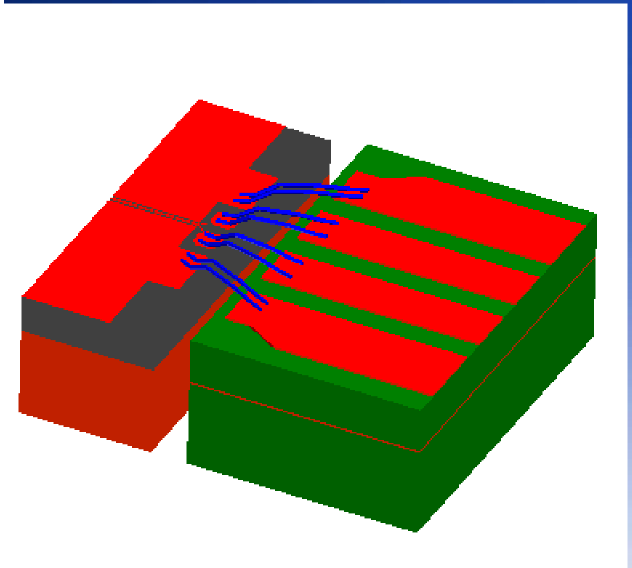
Cavity Depth and Different Signaling Conditions

- Chip thickness: 6mil
- Package shelf thickness: 22.1 mil
- Gap width: 6mil
- Bond wires diameter : 0.7 mil
- Edge bonding with 1 mil loop height
- No backside metal on-chip
- GCPW on package shelf
- Ceramic dielectric constant: 5.9





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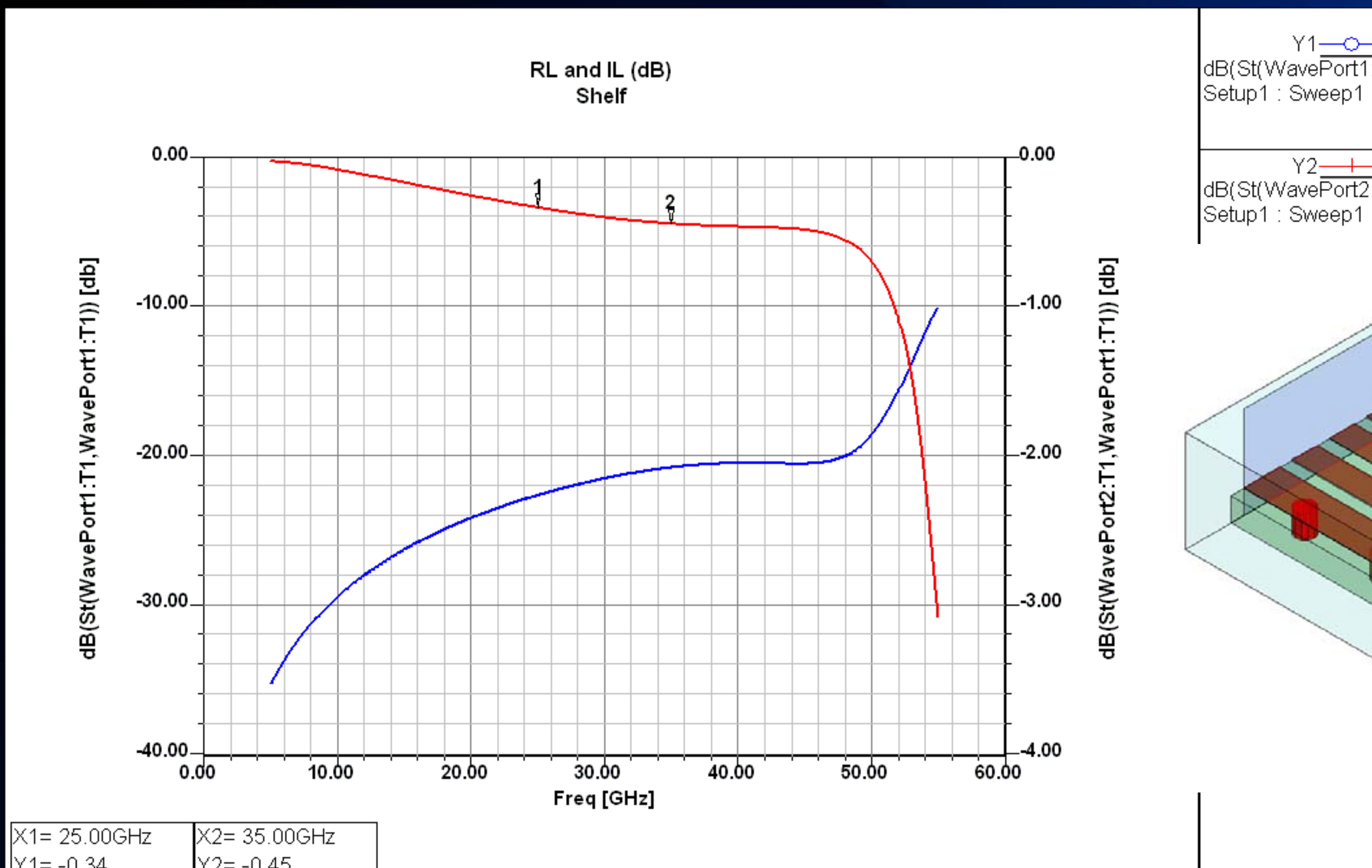
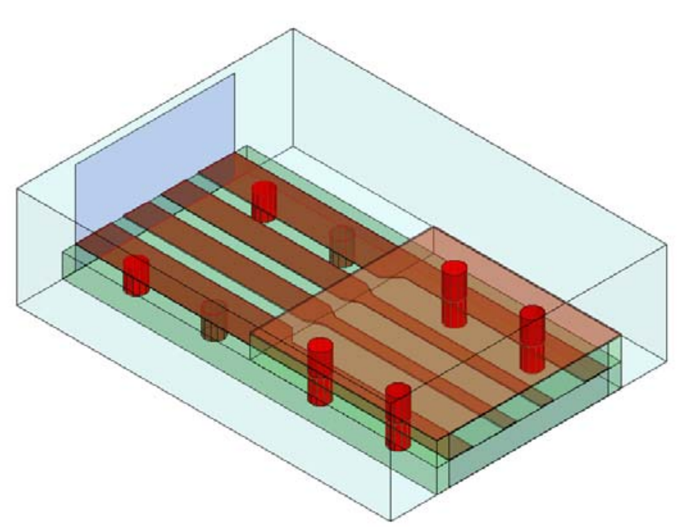
Transition at Package Shelf

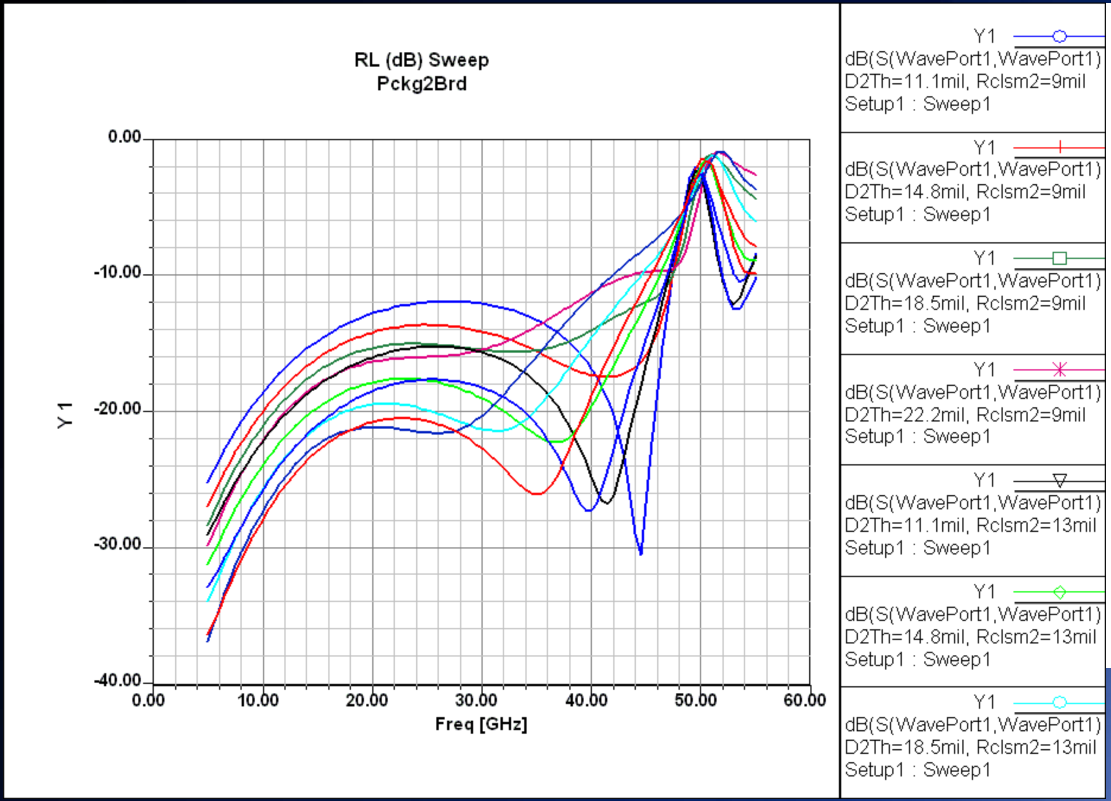
- Shielded coupled microstrip at package shelf
- Shielded coupled stripline to reach via at lands
- Transition length: 4mil

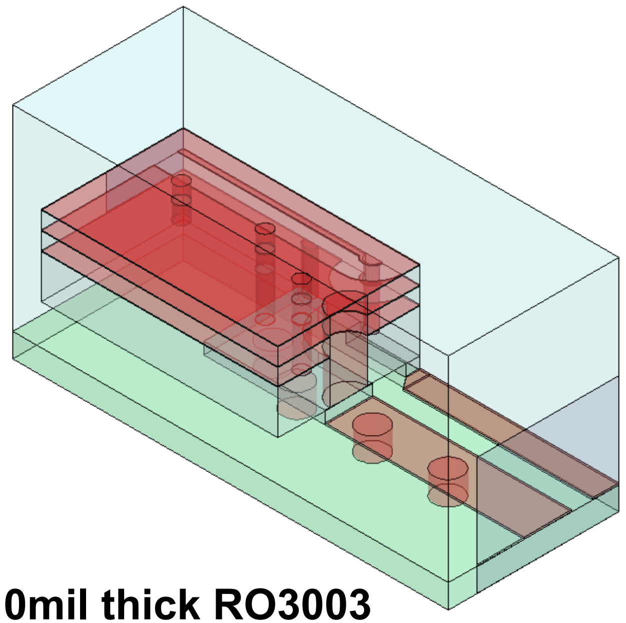




Transition to Board

- 10mil thick RO3003 board - shielded microstrip routing
- Optimization done sweeping several geometric parameters:
  - Thickness of LTCC tape
  - Radius of vias
  - Radius of clearance around signal via
  - Shape and size of signal land and ground land





10mil thick RO3003

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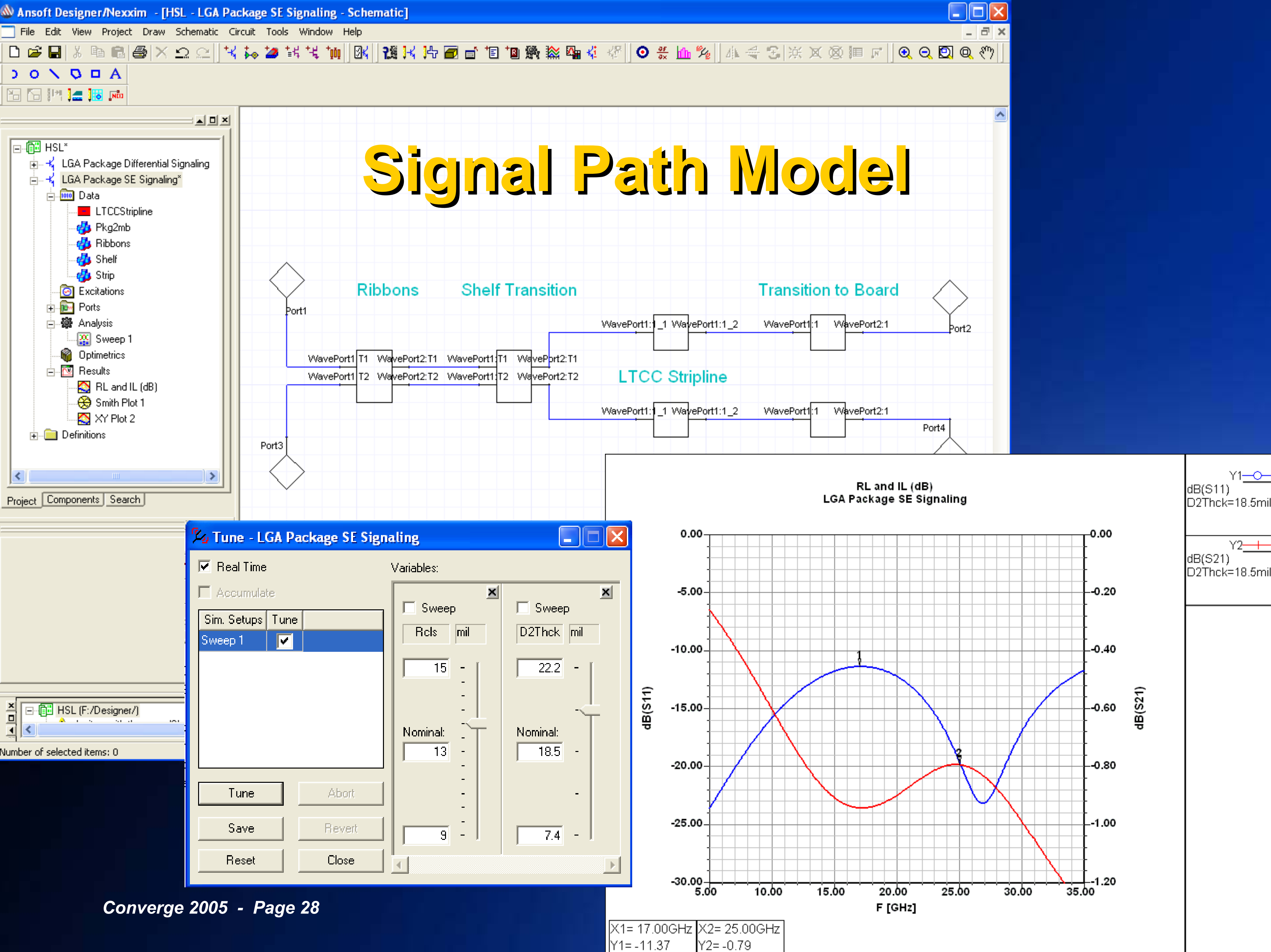
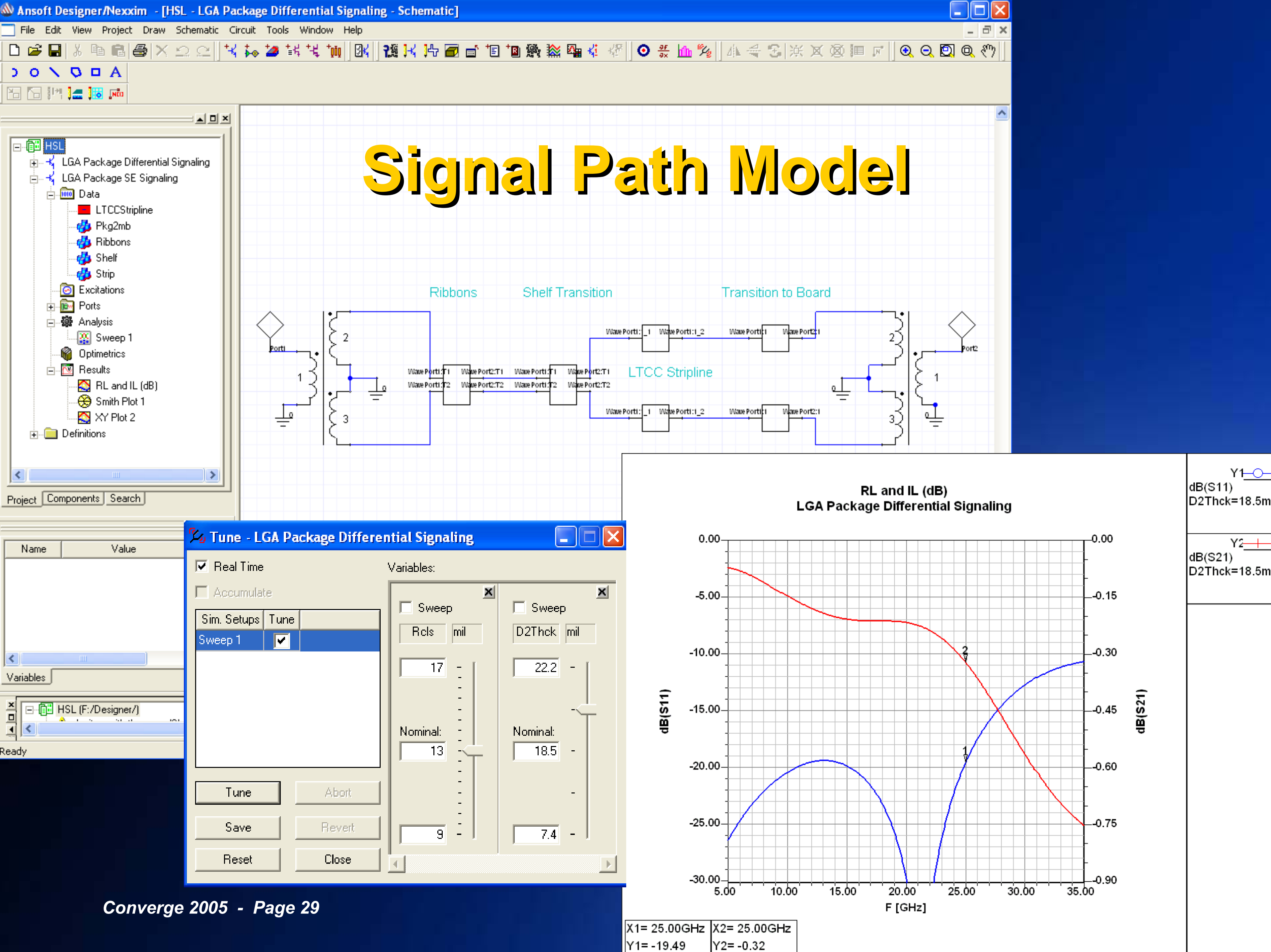
Signal Path Model

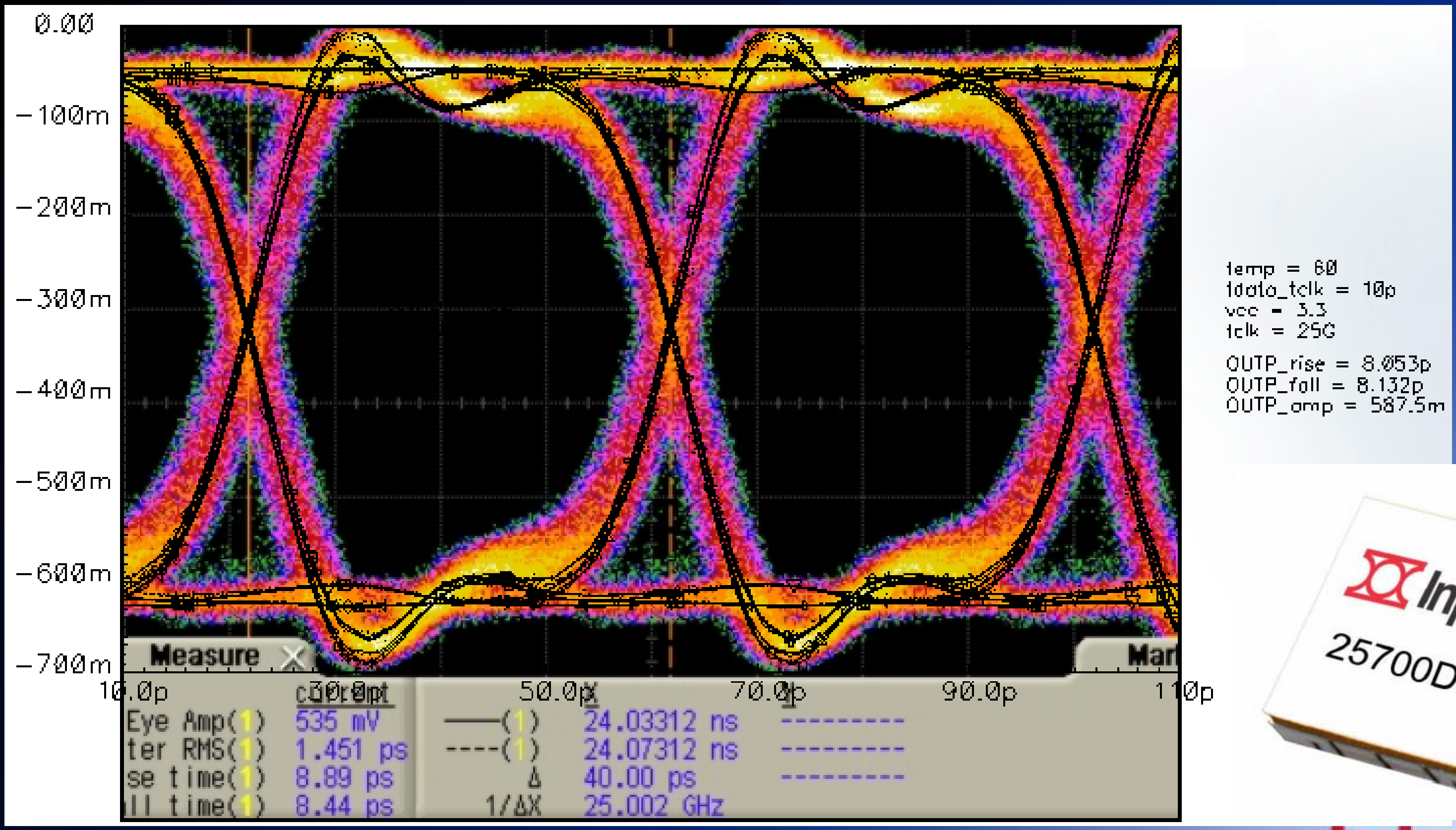


Signal Path Model



IC-Package Co-Simulation

- Time domain simulation wit actual IC driver is last step
  - Measured rise and fall time of 8.89ps and 8.44ps, jitter 1.45ps
  - Simulated rise and fall does not take into account traces on board, connectors



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Conclusions

- 3D Full-wave EM simulations is an enabling technology for the design of broadband surface mount packages
- Accurate 3D EM simulations cut design iterations and cost, shortening product development cycle.
- IC-package co-design is essential for first time success of high performance broadband devices.

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